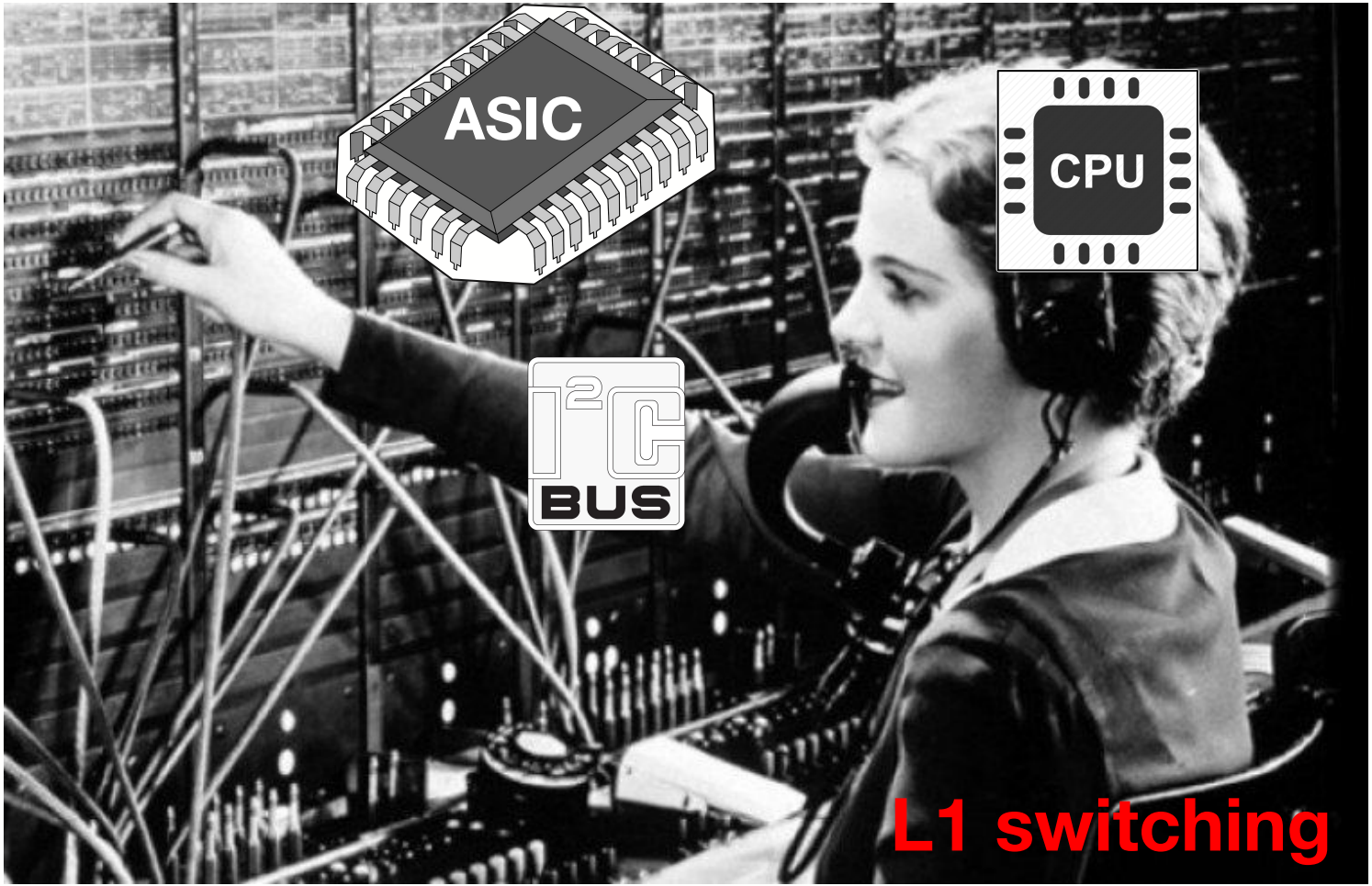
Layer 1 Switching

Arista 7130, FPGAs and the applications

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Agenda

- Layer 1 “switching”
- 7130 Overview
- FPGA Applications
  - Metamux - low latency multiplexing
  - Metawatch - high precision timestamping
  - MetaProtect - ACL Filtering
  - MultiAccess - Mux + Filter
- Use Cases
  - Ultra Low Latency switching
  - High Frequency Trading
  - Tap / TapAgg
  - Ultra Precise Timestamping
  - Media Conversion
  - Remote patch panel
  - Statistics
  - Custom FPGA Apps

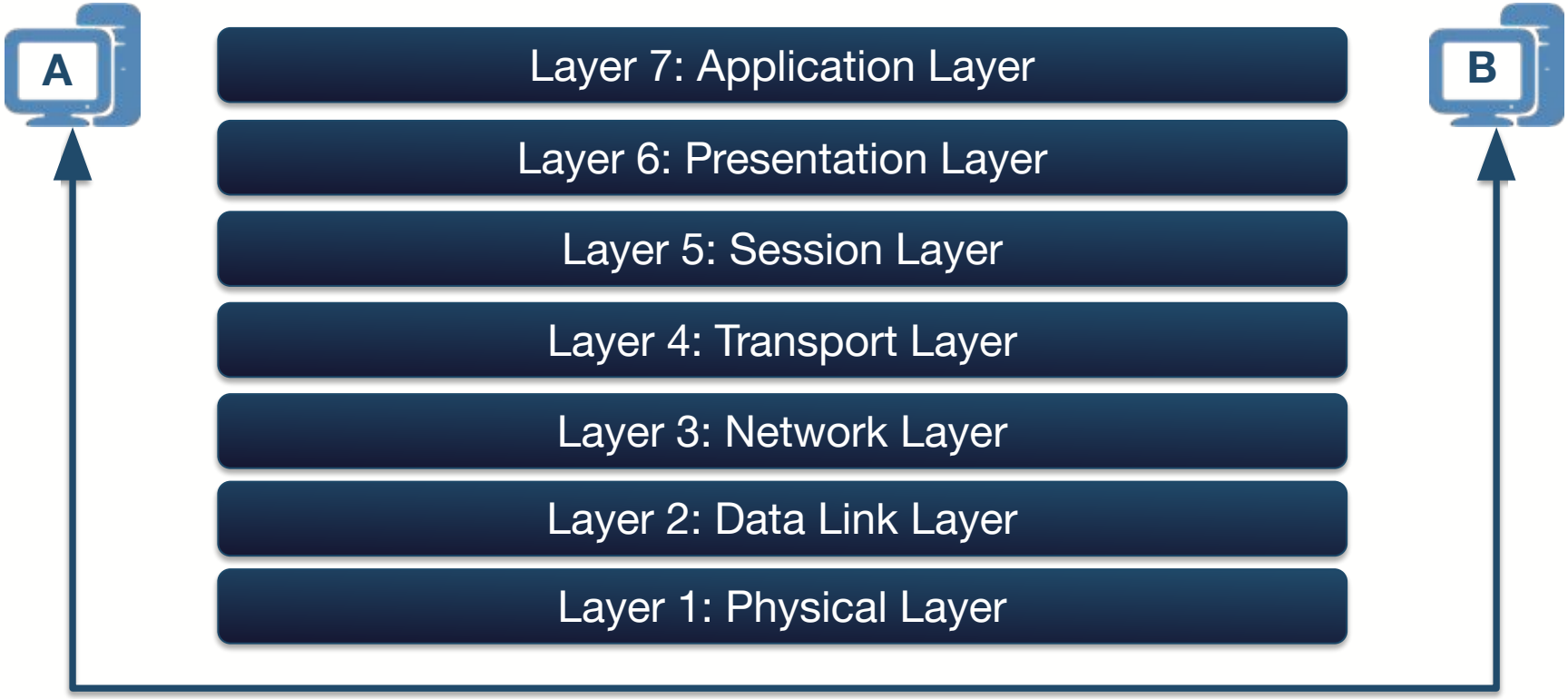
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L1 Switching

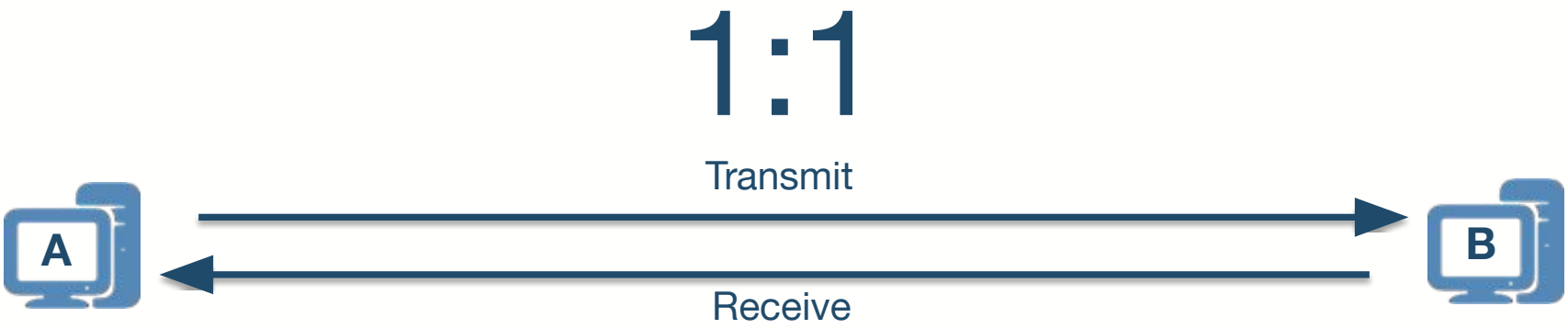
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Communication Stack



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What can you do at layer 1?



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What can you do at layer 1?



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Why can’t we do N:1 at Layer 1?



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Arista 7130 Overview

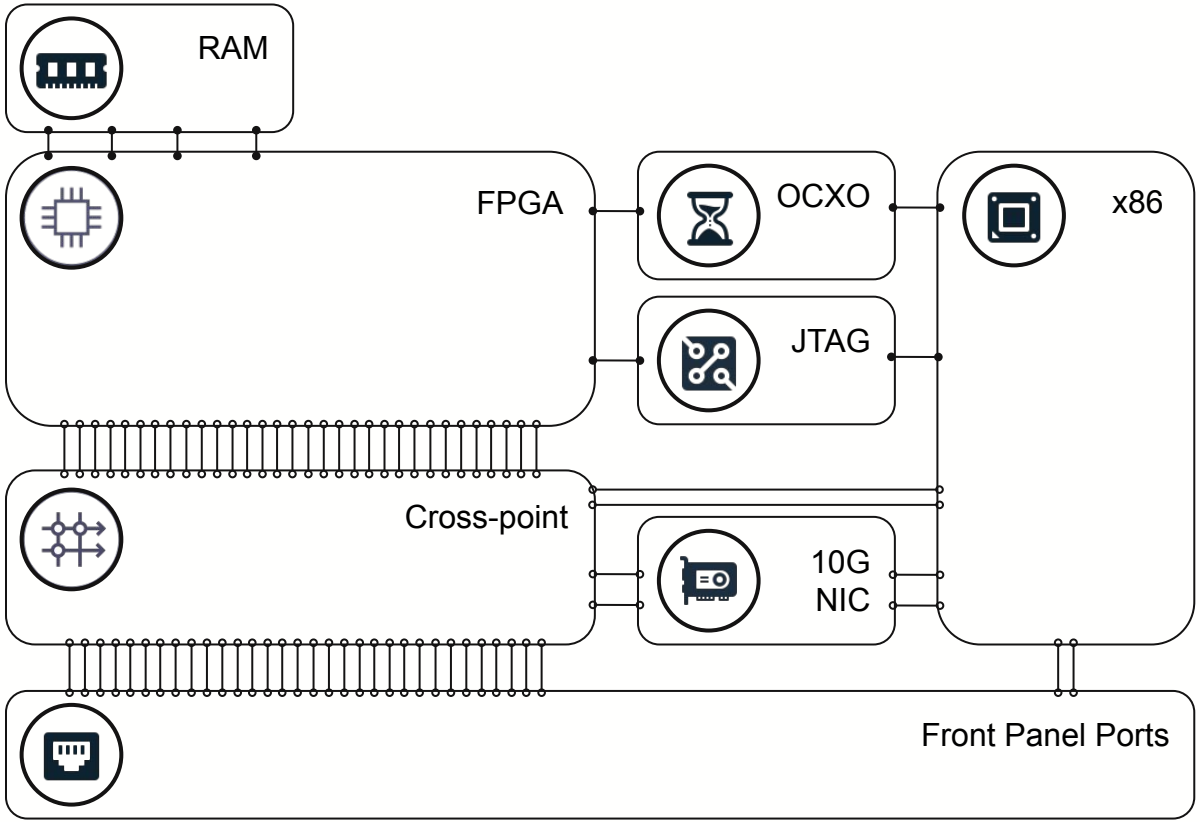
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Quick Intro...

- Previously Metamako
  - Founded in May 2013
  - Acquired by Arista in September 2018
- Now Arista 7130 Series
  - Financial Sector
  - High Frequency Trading
  - Remote patching / TAP
  - FPGA based applications

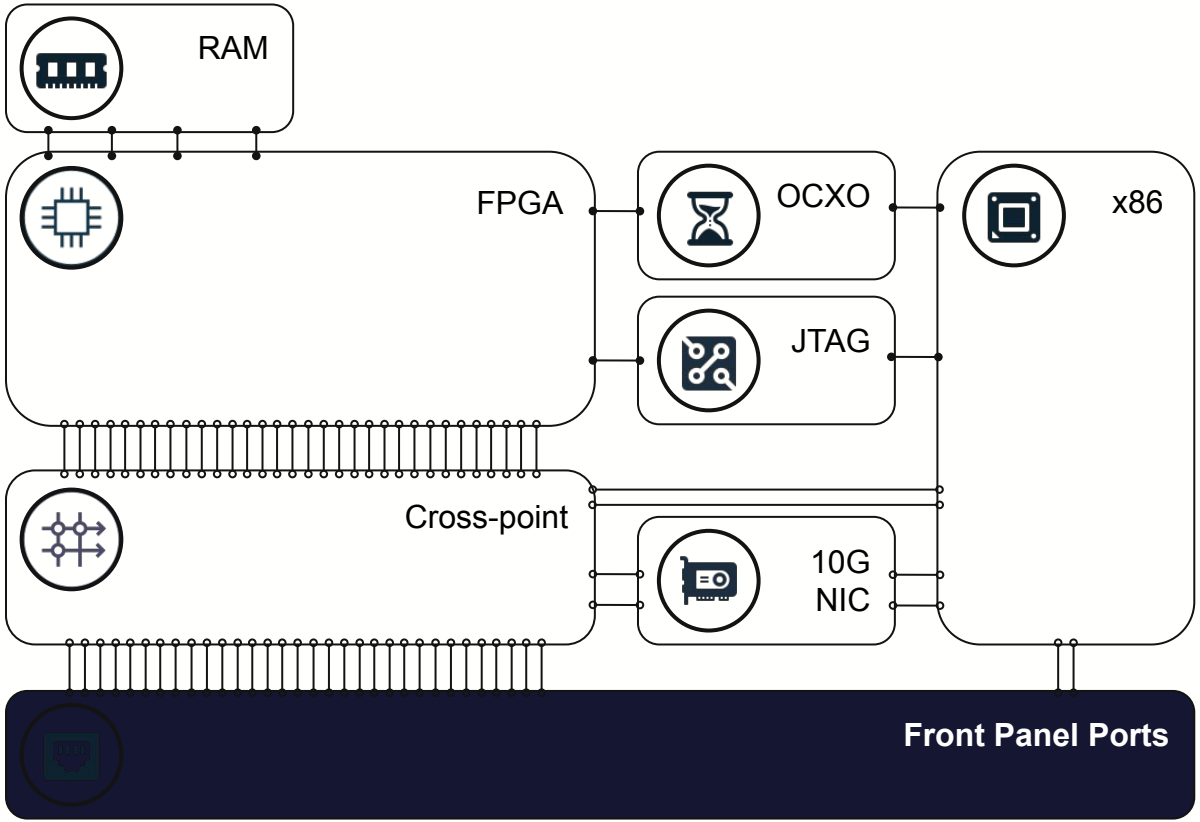
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Arista 7130 Architecture



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Arista 7130 Architecture

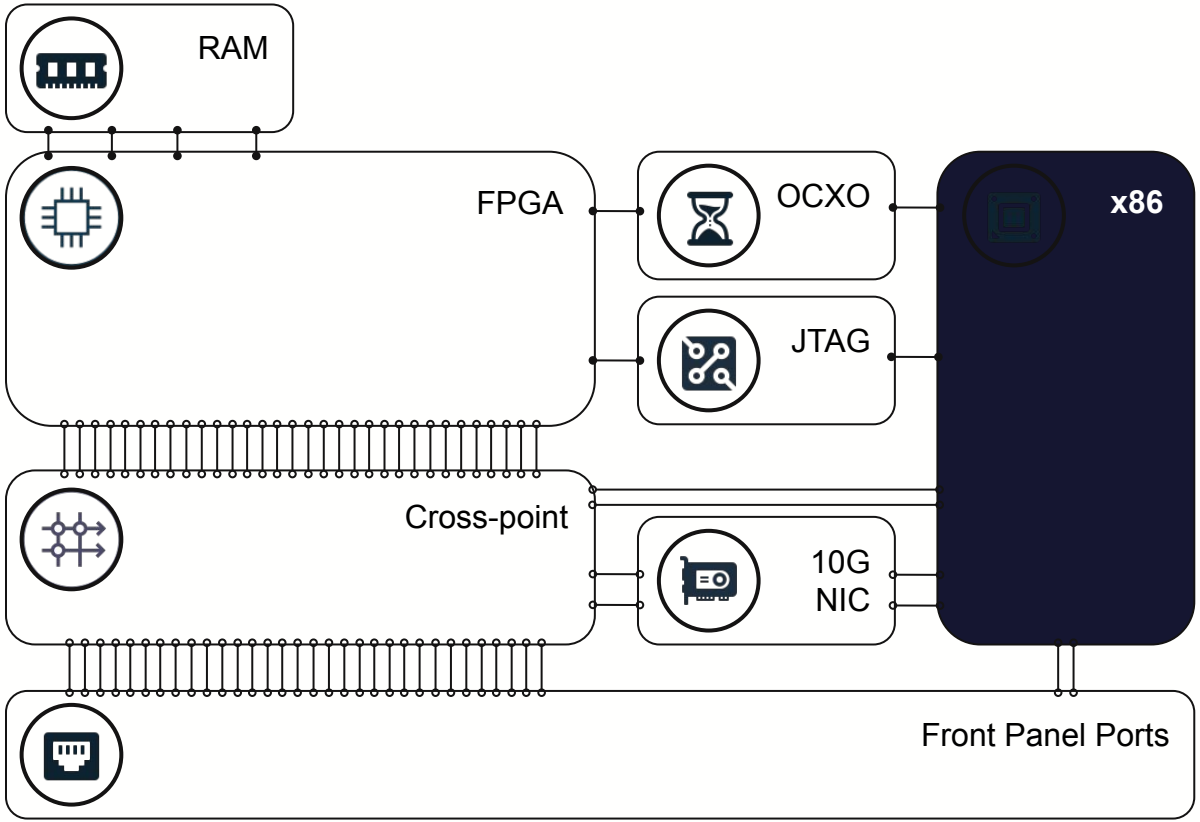


Front Panel Ports

- 10Gbe SFP+ port
- 16 Port (1RU)
- 32 Port (1RU)
- 48 Port (1RU)
- 96 Port (2RU)

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Arista 7130 Architecture

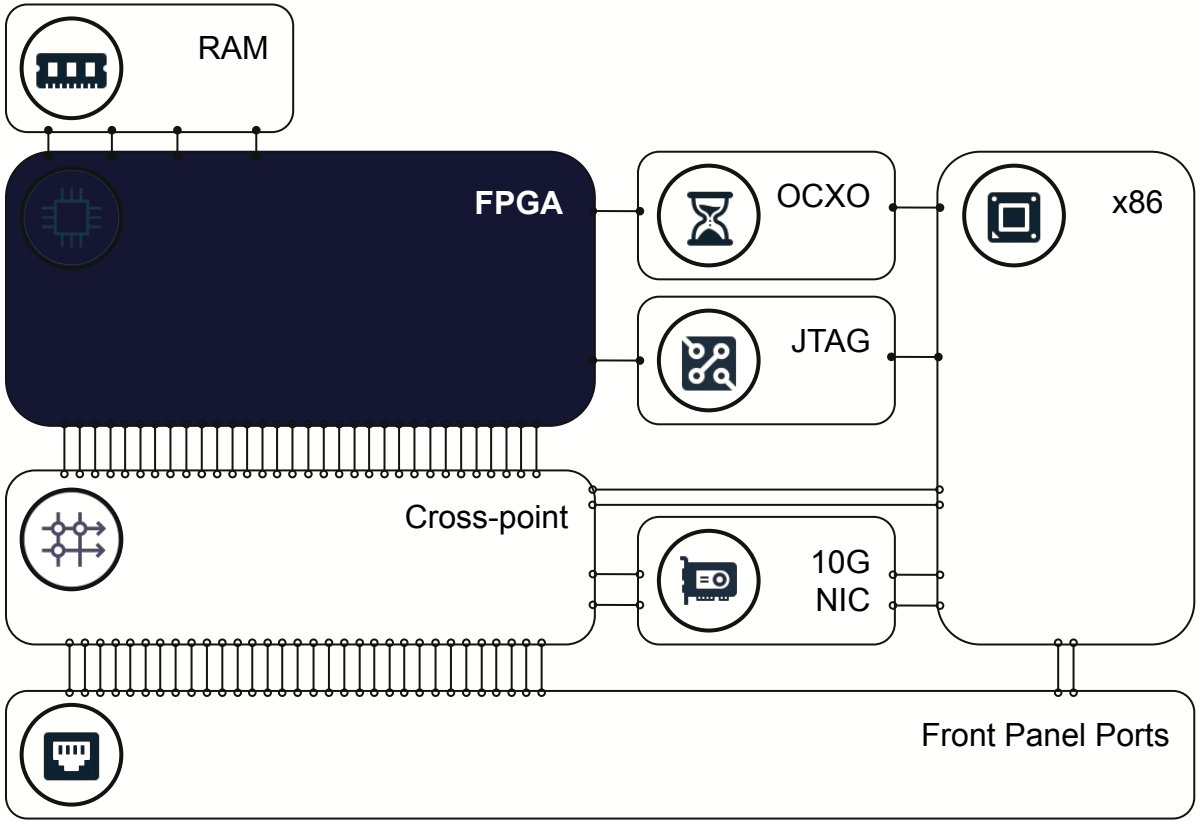


x86 Management Processor

- Intel Rangeley (Atom family)
- MOS - the management platform (linux based)
- Packet stats, etc.
- Ethernet command and control of FPGA
- PCIE

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Arista 7130 Architecture

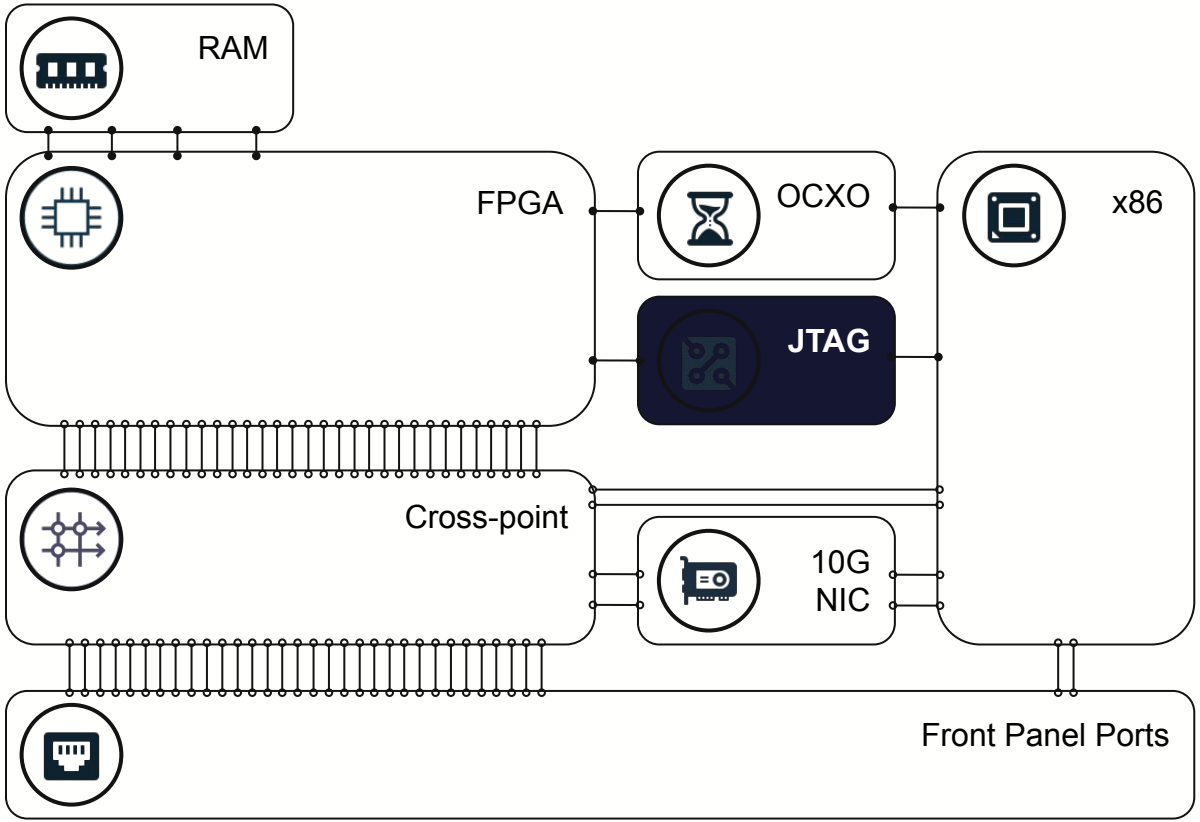


FPGA

- 60/58 transceivers connected to cross-point (L-Series)
- Xilinx UltraScale+ VU7P-2 (L)
- Xilinx UltraScale+ VU9P-3 (LB)
- Fully user programmable
- Standard applications available from Arista

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Arista 7130 Architecture

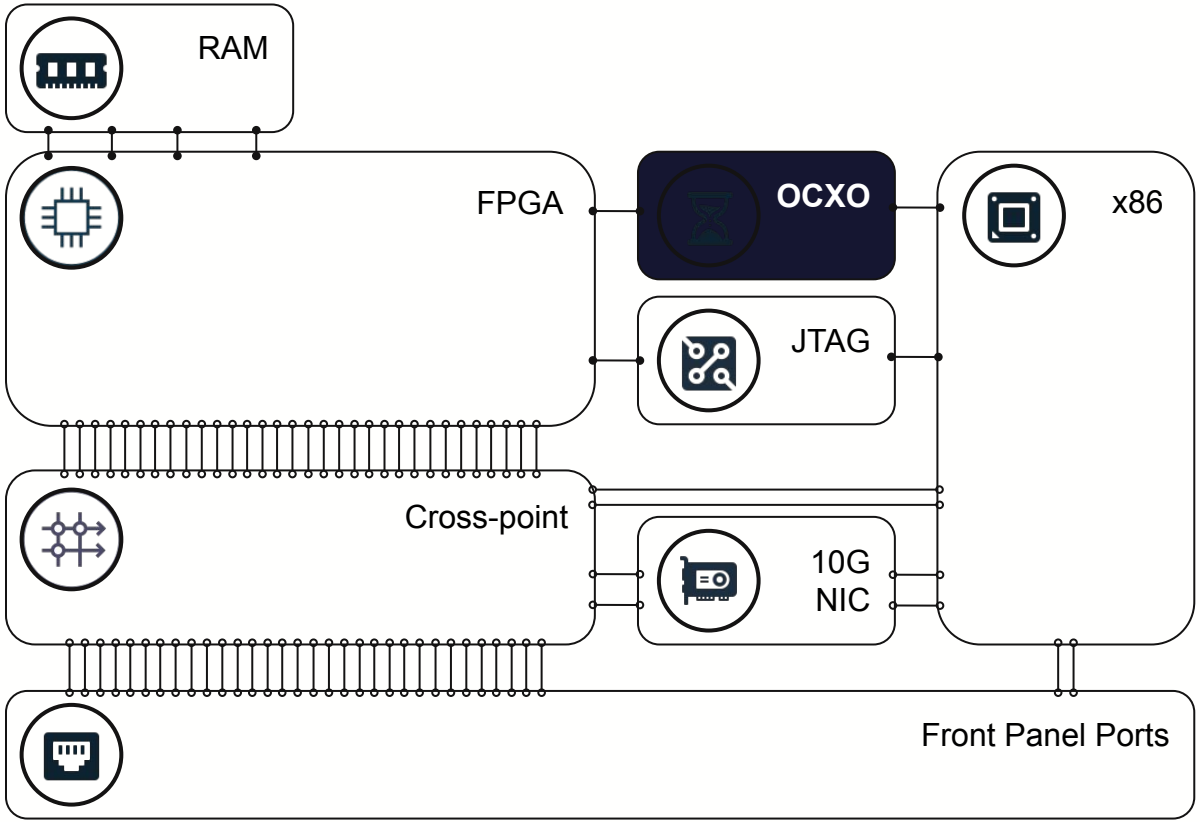


JTAG

- Allows remote reprogramming of FPGA chip
- Leverage existing FPGA development tools remotely

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Arista 7130 Architecture

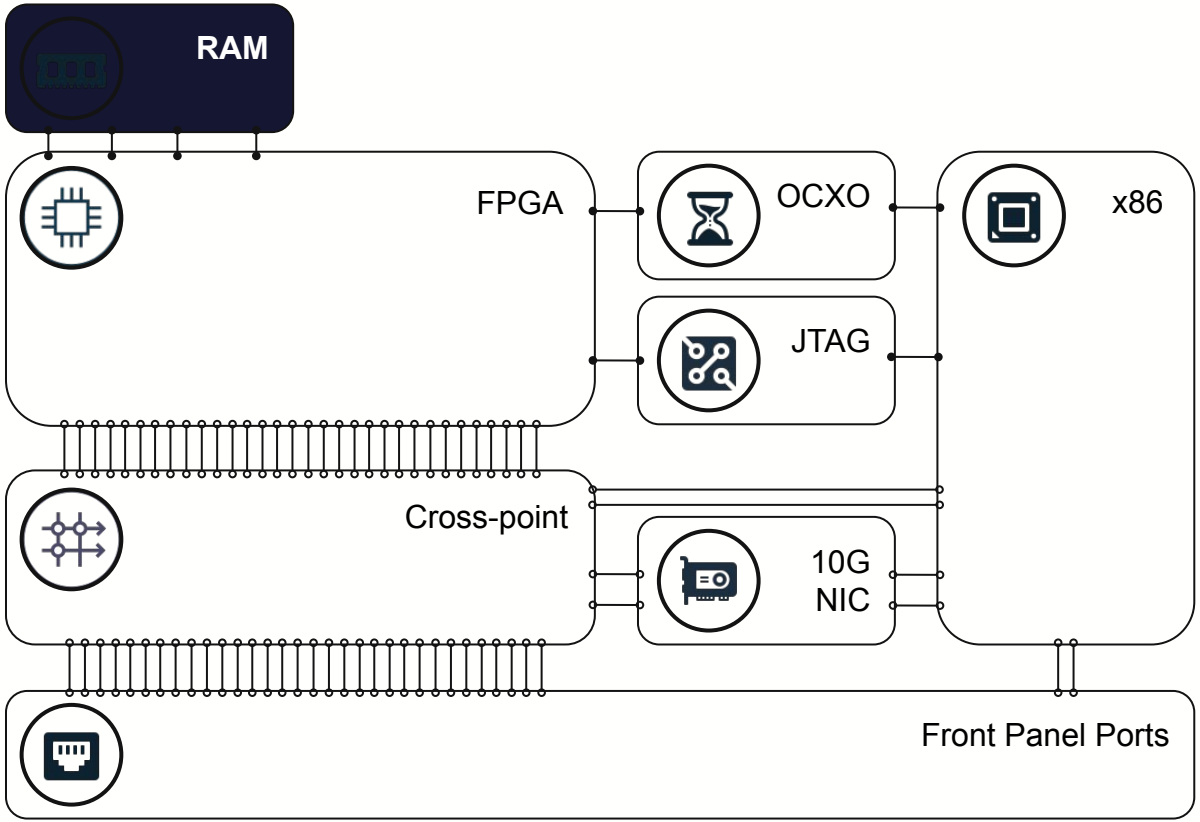


Precision OCXO Clock

- Precision clock provides a stable reference for MetaWatch or your own applications.
- 10MHz OCXO standard on 7130L/7130LB
- Optional Atomic clock & GPS

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Arista 7130 Architecture

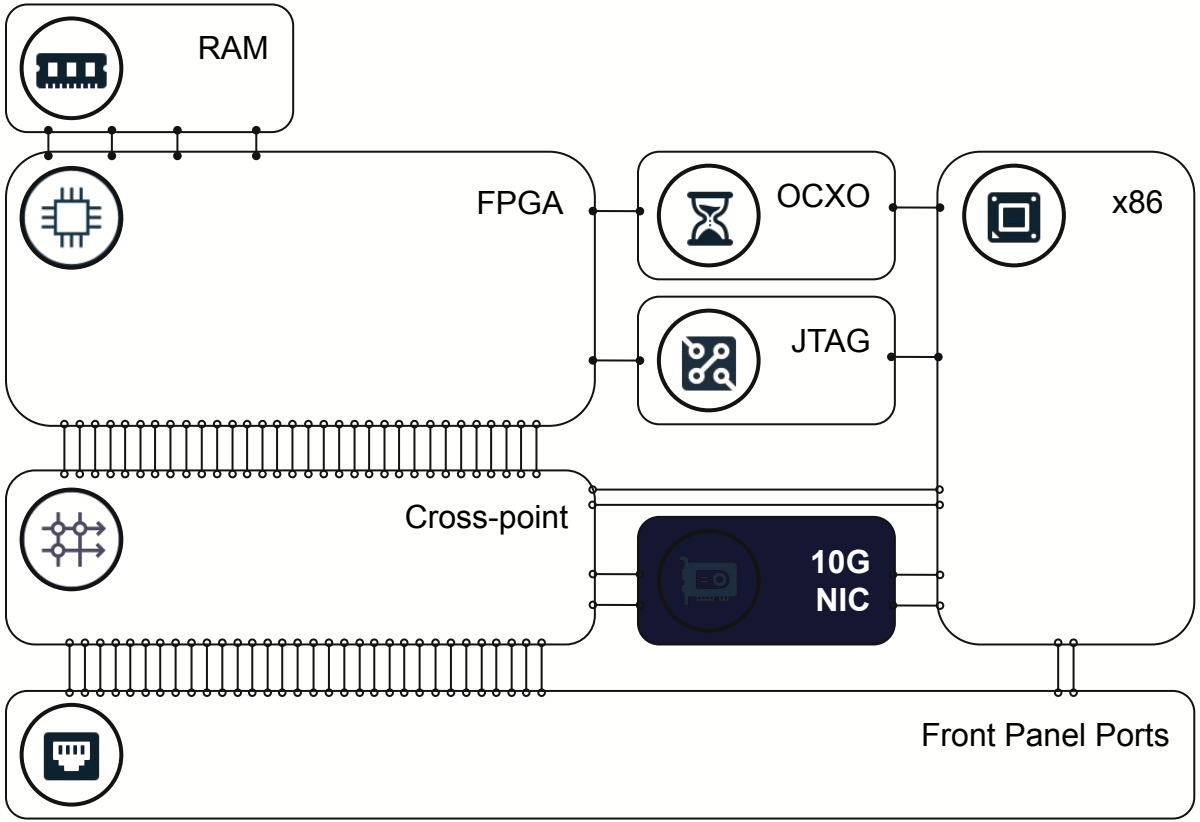


RAM

- Off chip RAM for use within FPGA applications
- We use it for deep buffering
- 4 x 8GB DDR 2400 ECC

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Arista 7130 Architecture

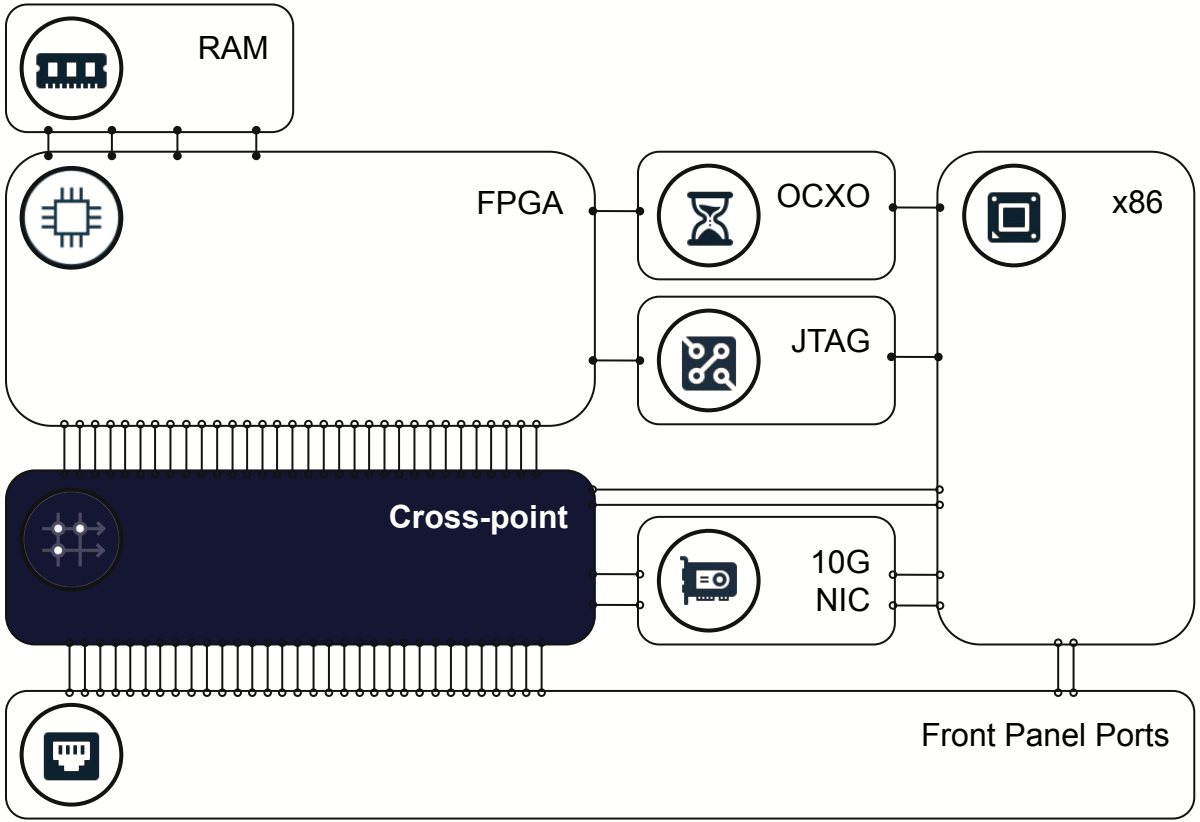


10G Management NIC

- Onboard 2X10G offload NIC for “fast path” to CPU based applications
- Command and control
- BGP/PIM for MetaMux

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Arista 7130 Architecture



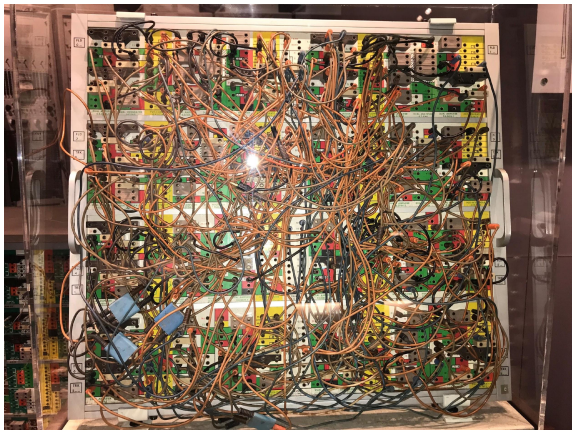
Cross-point

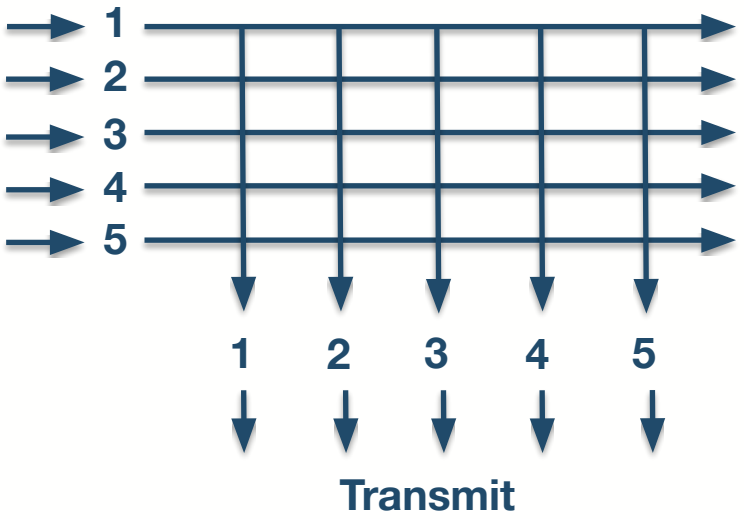
- Up to 10G connectivity between all components
- Port mirroring
- Replication

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Arista 7130: Layer 1 Cross-point

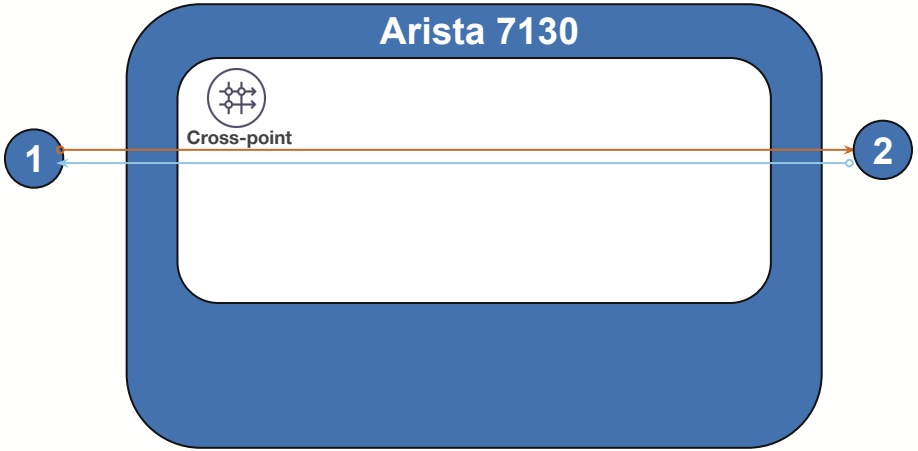
- All ports are bi-directional
- Each port can be configured to transmit what's received on any other port
- Forwarded at the bit level
- Possible to transmit one-to-many for broadcast applications

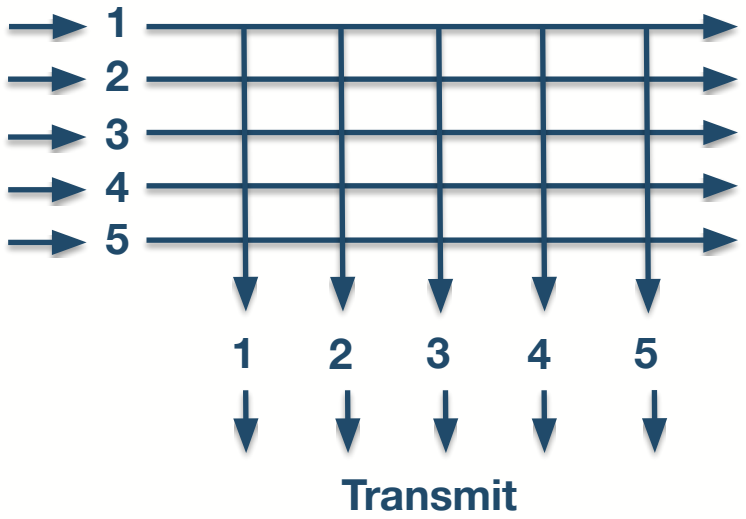




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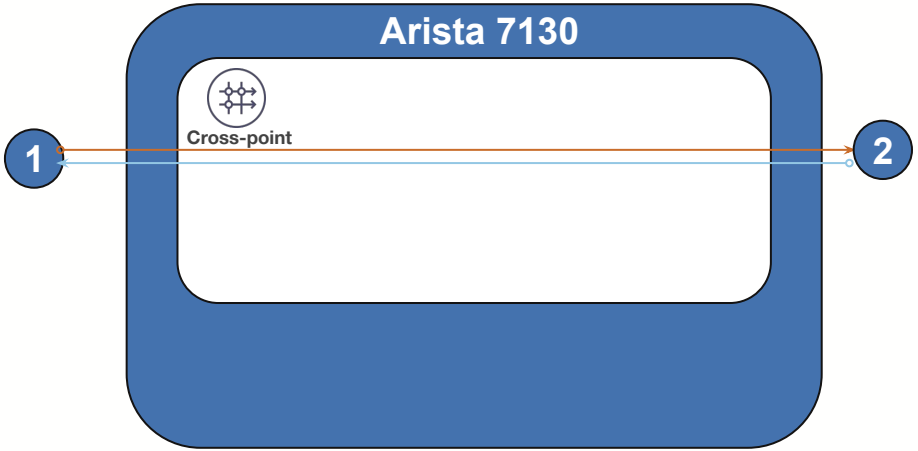
Arista 7130: Patch panel (1:1)



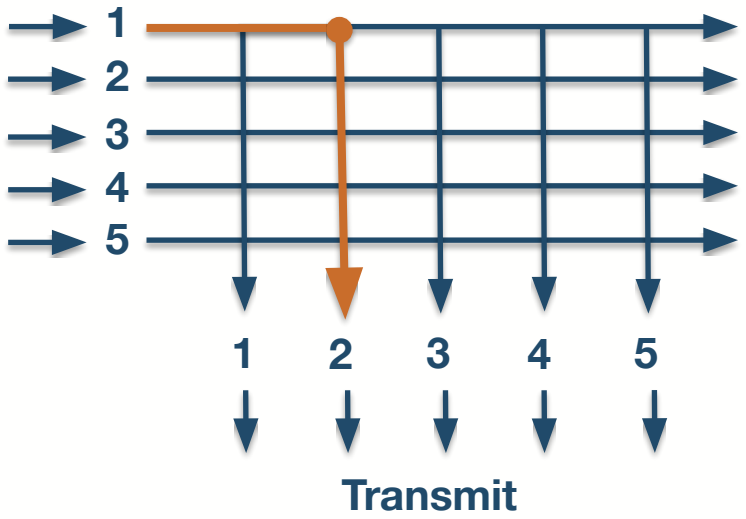


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Arista 7130: Patch panel (1:1)

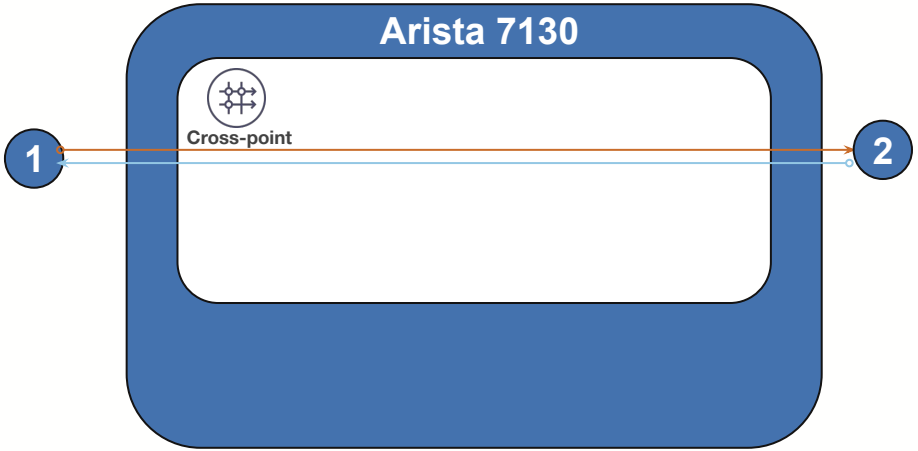



```
hostname(config)> int et2
hostname(config-if-et2)> source et1
```

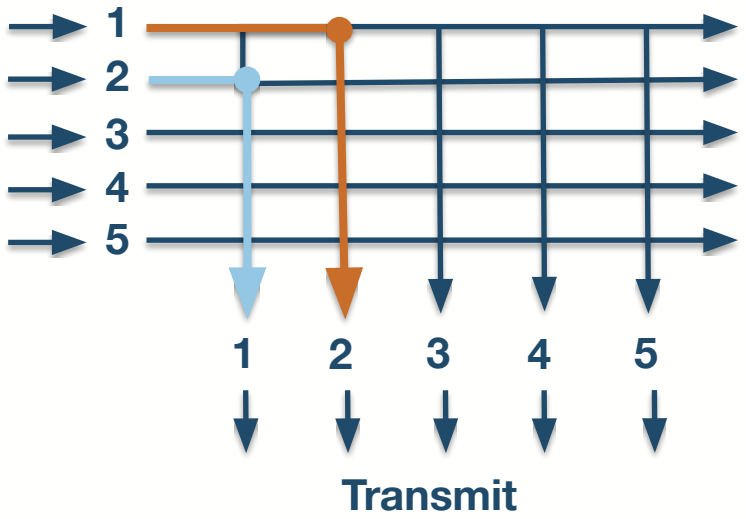


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Arista 7130: Patch panel (1:1)

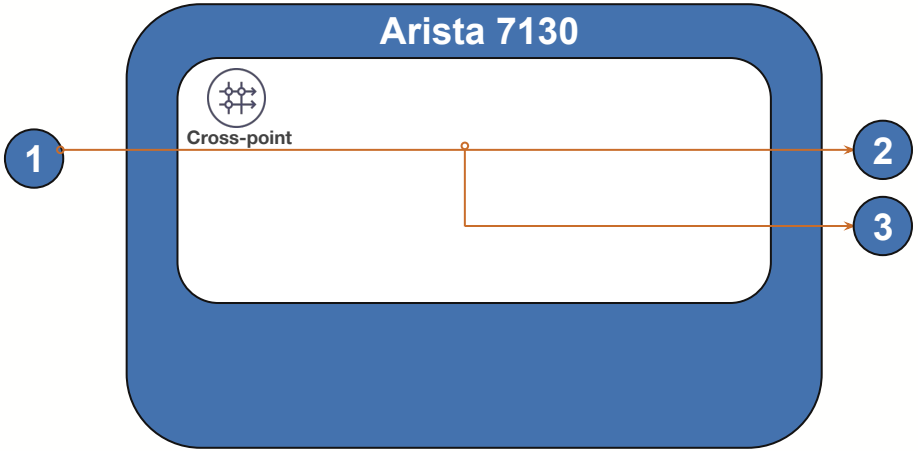



```
hostname(config)> int et2
hostname(config-if-et2)> source et1
hostname(config)> int et1
hostname(config-if-et1)> source et2
```

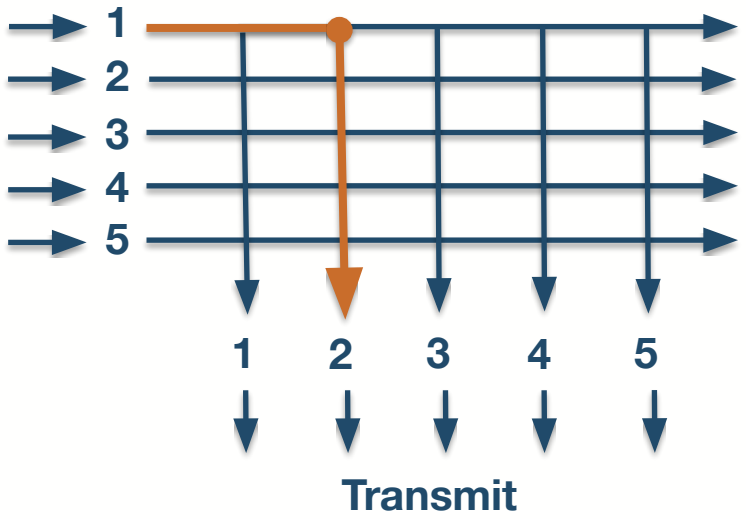


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Arista 7130: Replication (1:N)

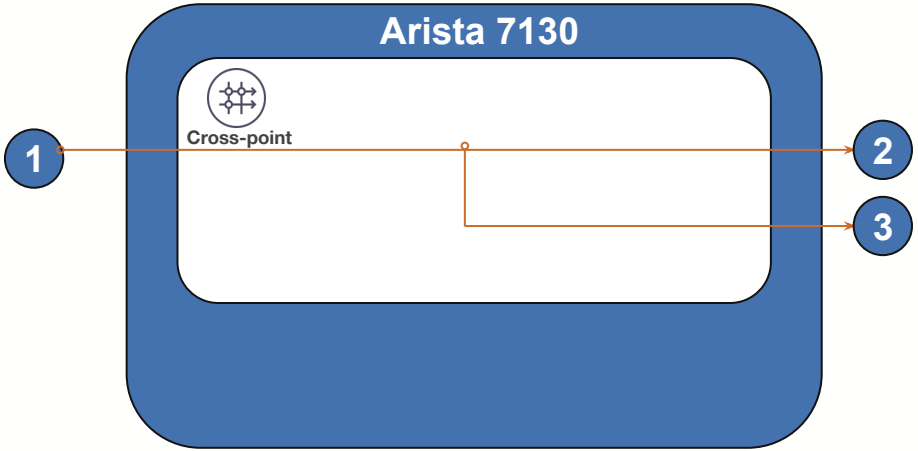



```
hostname(config)> int et2
hostname(config-if-et2)> source et1
```

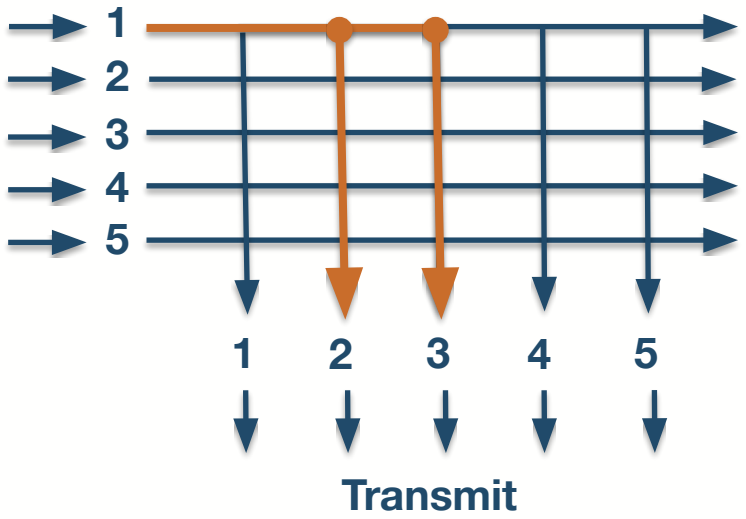


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Arista 7130: Replication (1:N)

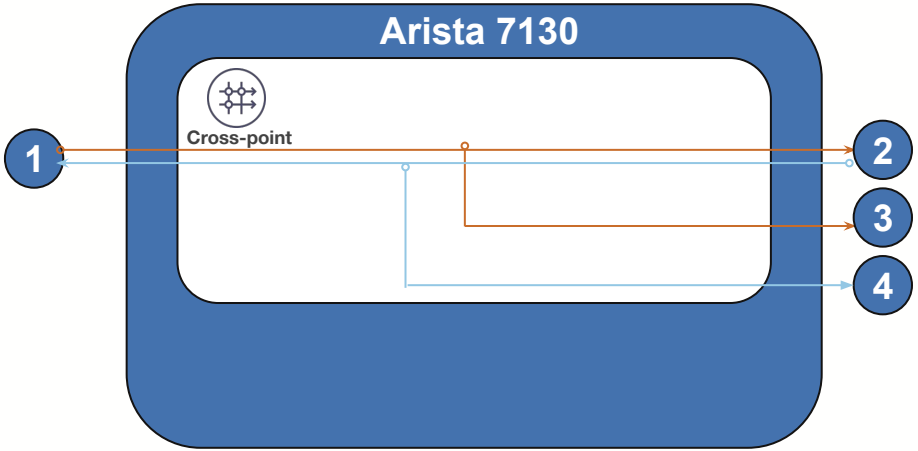



```
hostname(config)> int et2
hostname(config-if-et2)> source et1
hostname(config)> int et3
hostname(config-if-et3)> source et1
```

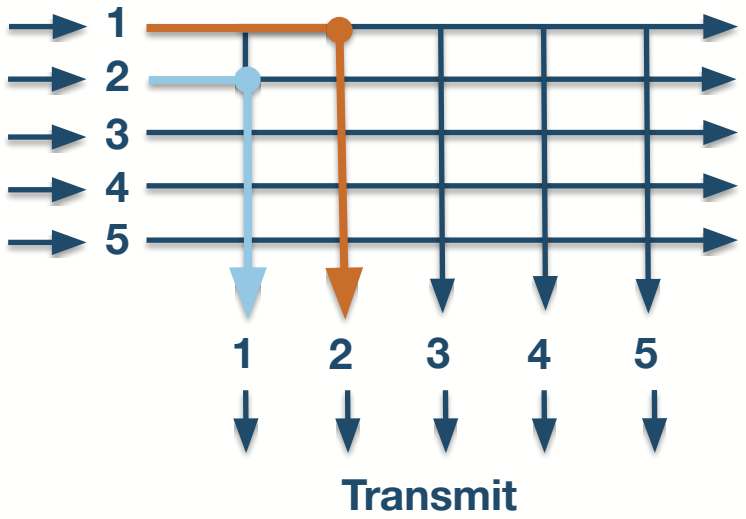


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Arista 7130: Tapping a bi-directional link (1:1 + 1:N)

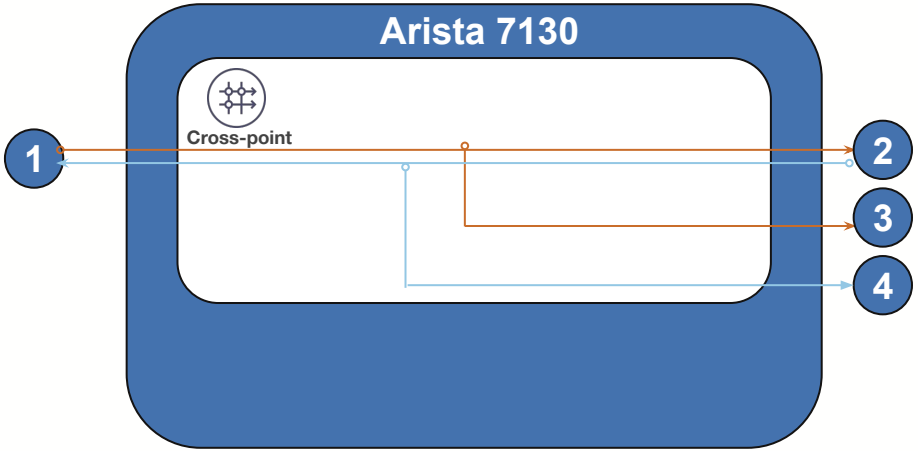



```
# create bi-directional link (patch)
hostname(config)> int et2
hostname(config-if-et2)> source et1
hostname(config)> int et1
hostname(config-if-et1)> source et2
```

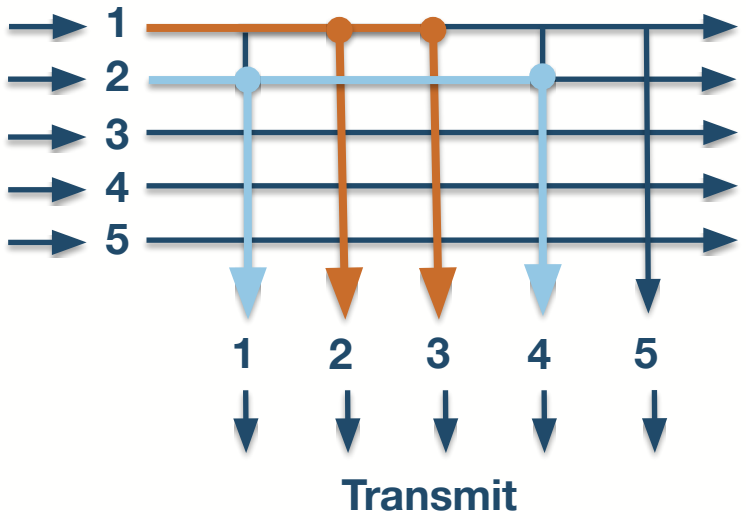


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Arista 7130: Tapping a bi-directional link (1:1 + 1:N)




```
# replicate (tap) to ports #3 #4
hostname(config)> int et3
hostname(config-if-et3)> source et1
hostname(config)> int et4
hostname(config-if-et4)> source et2
```



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Arista 7130: Latency

Arista 7130-48 port to port latency

4 nanoseconds

Faster than a meter of fiber

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Arista 7130 **Connect** Series

- A fully featured **layer 1+** switch
- 16, 48, or 96 port devices
  - Unrestricted 1:1 or 1:N
  - Port replication/mirroring/tapping
  - Bit for bit forwarding
  - Non-blocking
  - 1RU or 2RU
  - Dual power supply/fans
    - Configurable air flow
    - AC or DC



DCS-7130-16#: Arista 7130 Series Connect 16 Layer-1 Switch
DCS-7130-48#: Arista 7130 Series Connect 48 Layer-1 Switch
DCS-7130-96#: Arista 7130 Series Connect 96 Layer-1 Switch

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Arista 7130 **Connect** Series

- What is **layer 1+**?
  - Signal regeneration (EDC/CDR)
  - Per port packet statistics
    - valid packets, invalid packets, link state
  - Eye diagram for monitoring and troubleshooting signal quality
  - Ports can be “sniffed” via the management system (e.g. tcpdump)
  - Fully managed SFP+ interface diagnostics including light levels, temperature and voltages
  - Media Conversion (e.g. fibre to DAC, single mode to multimode)
  - Dynamic Patching/Link Management
  - Supports many standards: SNMP, LLDP, InfluxDB, JSON RPC, NetConf, Syslog, AAA



DCS-7130-16#: Arista 7130 Series Connect 16 Layer-1 Switch
DCS-7130-48#: Arista 7130 Series Connect 48 Layer-1 Switch
DCS-7130-96#: Arista 7130 Series Connect 96 Layer-1 Switch

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Arista 7130 models with FPGA

NEW L-Series

- 1x Xilinx Virtex® UltraScale+™ VU7P “L”
- 1x Xilinx Virtex® UltraScale+™ VU9P “LB”
- 32, 64 & 96 port models
- Optimized for MetaWatch or MetaMux

E-Series

- 1x or 3x Xilinx Kintex® UltraScale™ KU095
- 1x or 3x Xilinx Virtex® UltraScale+™ VU9P
- 32, 64 & 96 port models
- Optimized for MetaMux and MultiAccess

K-Series

- 1x Xilinx Virtex® 7 415T
- 32, 64 & 96 port models
- Optimized for MetaWatch

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FPGA Applications

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Where do FPGA's fit in?

- FPGA = Field Programmable Gate Array
- Reconfigurable hardware chip using software logic
- Typical uses:
  - ASIC prototyping
  - Digital signal processing
  - Device controllers
  - Cryptography
  - Financial trading applications
  - Media and entertainment

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Applications

MetaWatch – Advanced network monitoring



- Tapping
- Time synchronisation
- Picosecond-precise timestamping
- Deep buffering (32GB)
- Multi-port capture

Protect™ Firewall – Secure ACL-based filtering



- Filter latency of 112 nanoseconds
- Cut-through filtering with up to 510 rules per ACL
- Comprehensive logging

MetaMux – Low-latency multiplexing



- Data Aggregation in 45 nanoseconds
- Deterministic
- Packet Statistics

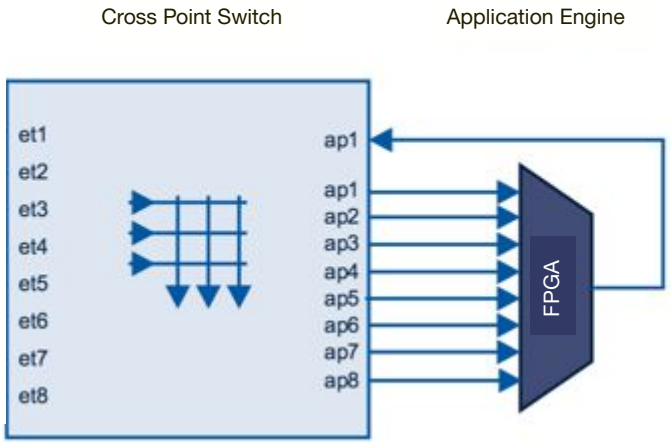
MultiAccess – Shared services



- MetaMux aggregation 95 nanoseconds
- Packet filtering in just 95 nanosecond
- Per port filters for different data subsets
- Deterministic

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FPGA Connectivity



Etx are front panel interfaces
ApX are FPGA interfaces

All interfaces are just Rx and Tx lanes to the CrossPoint
User defines mapping between EtX and ApX interfaces

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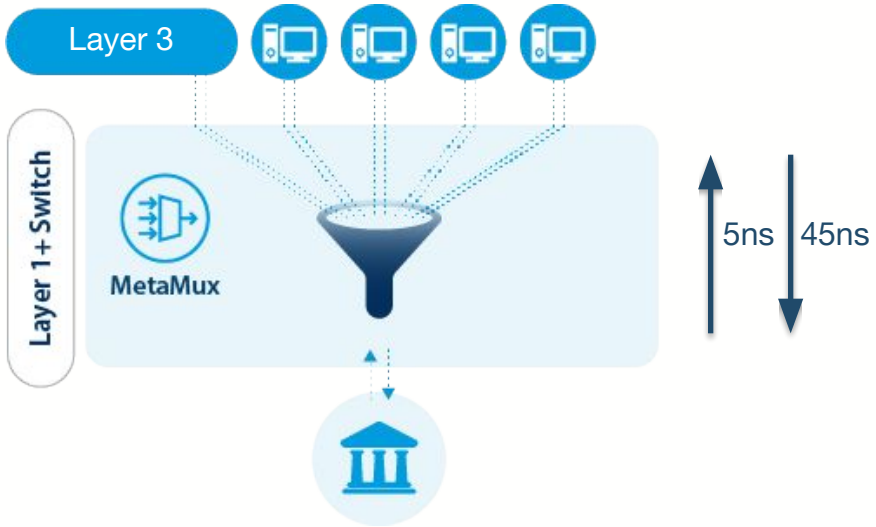


MetaMux

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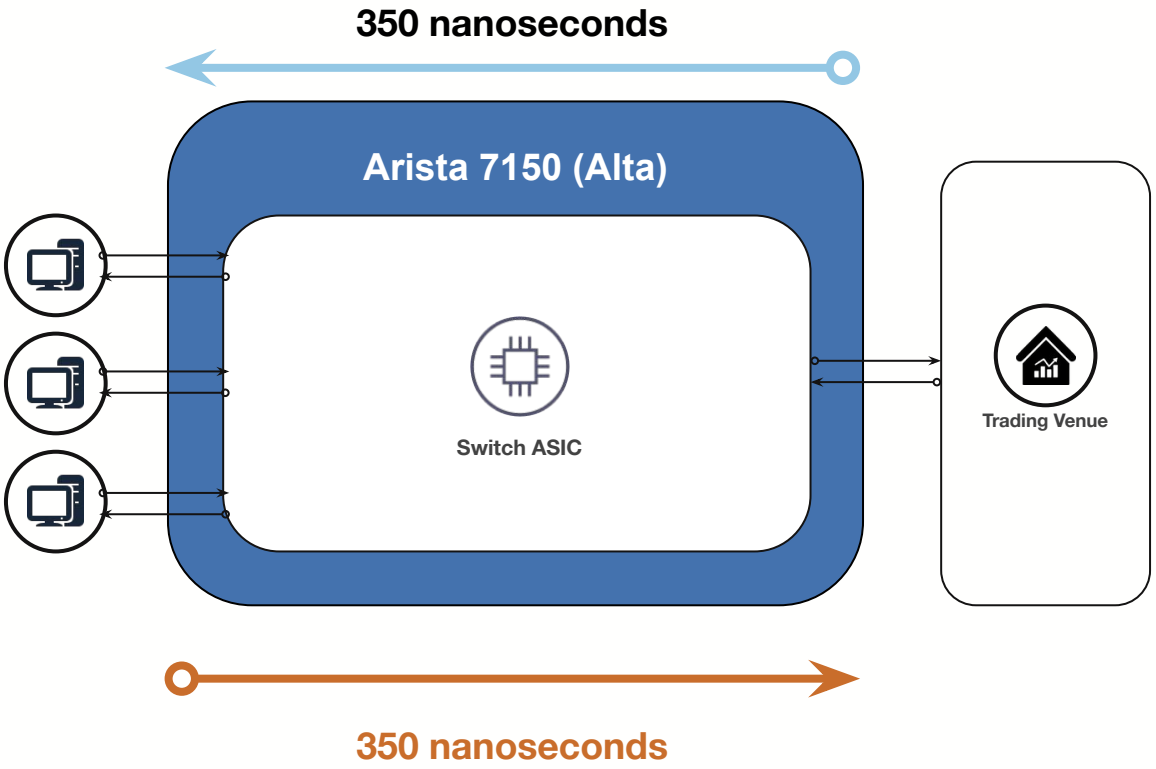
MetaMux: Low latency Muxing

- Optimized for the Arista 7130L & E Series
- Typically used for exchange facing low-latency trading
- Ultra-low latency:
  - 5 nanosecond pass-through latency
  - As low as 39 nanosecond multiplexing/aggregation
- Guaranteed determinism
- Complete packet statistics
  - Queue statistics



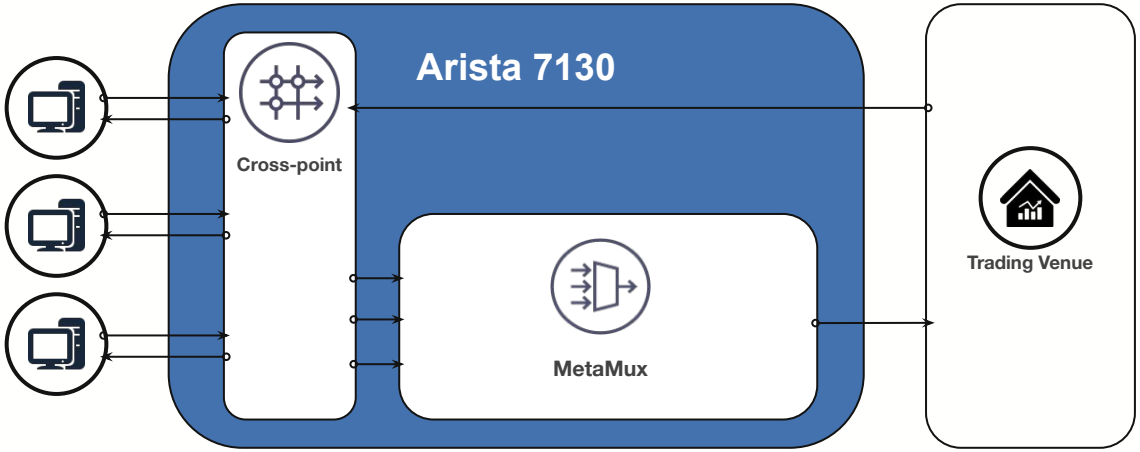
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Arista 7130: MetaMux Backstory



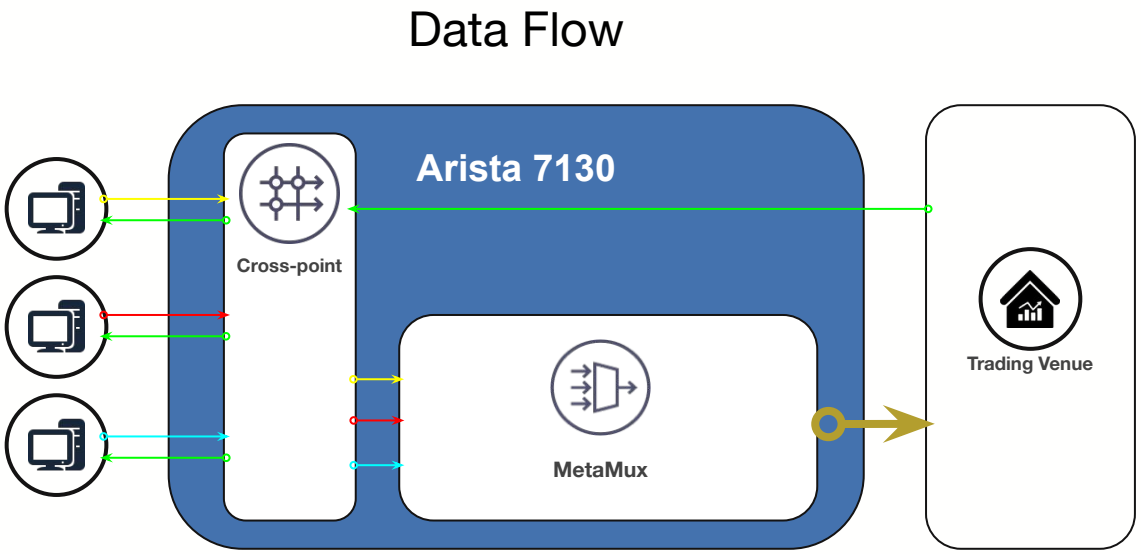
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Arista 7130: MetaMux



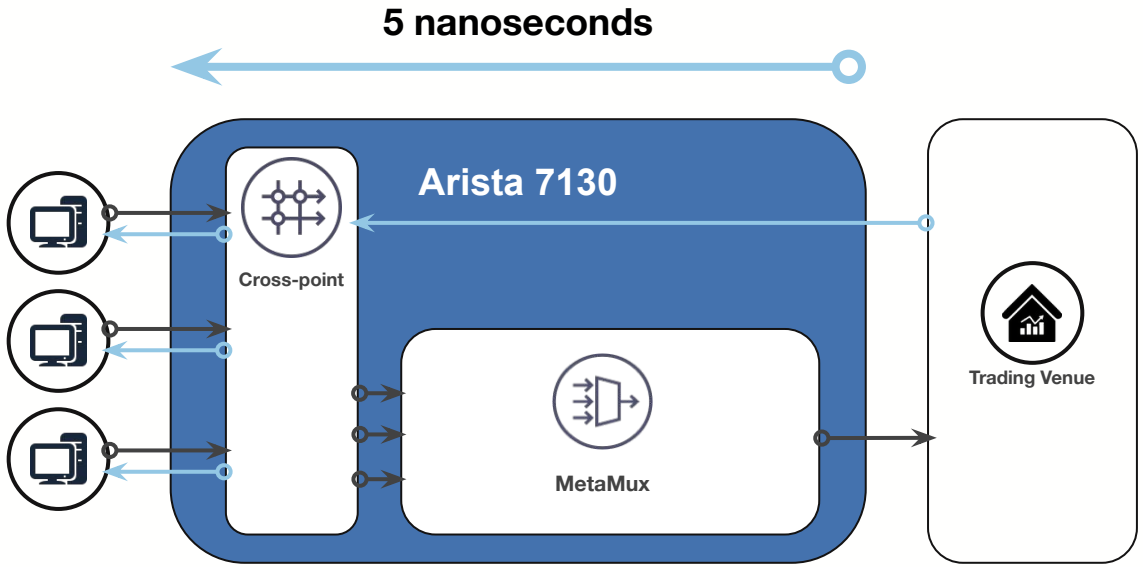
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Arista 7130: MetaMux



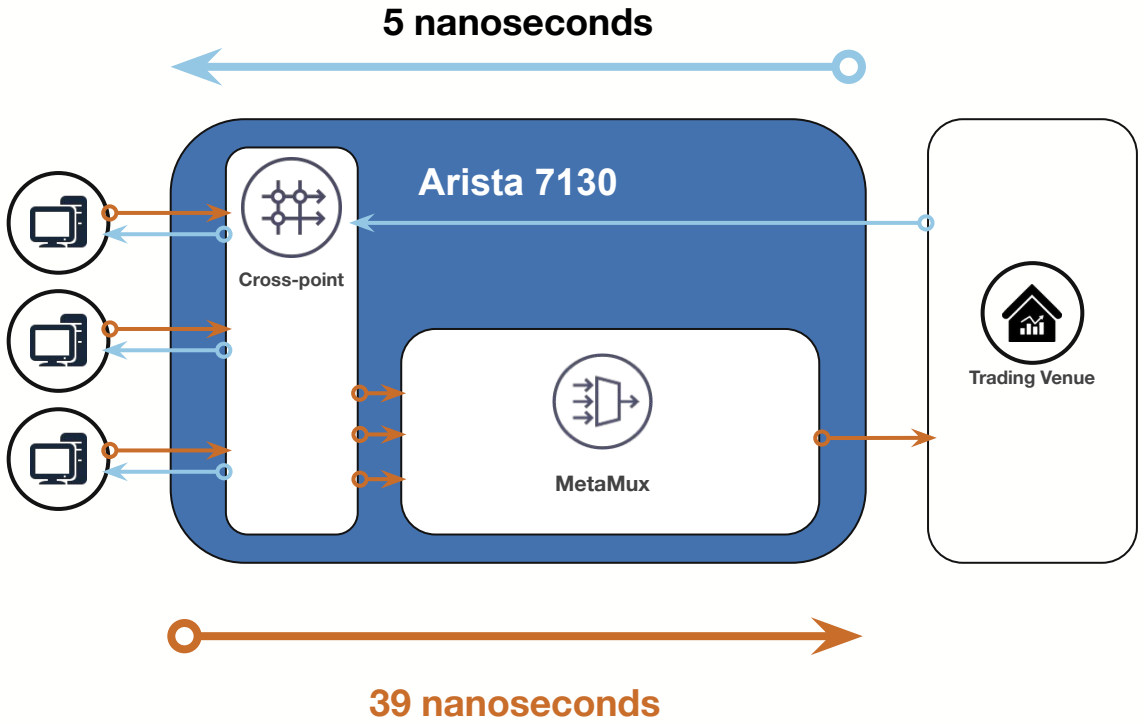
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Arista 7130: MetaMux



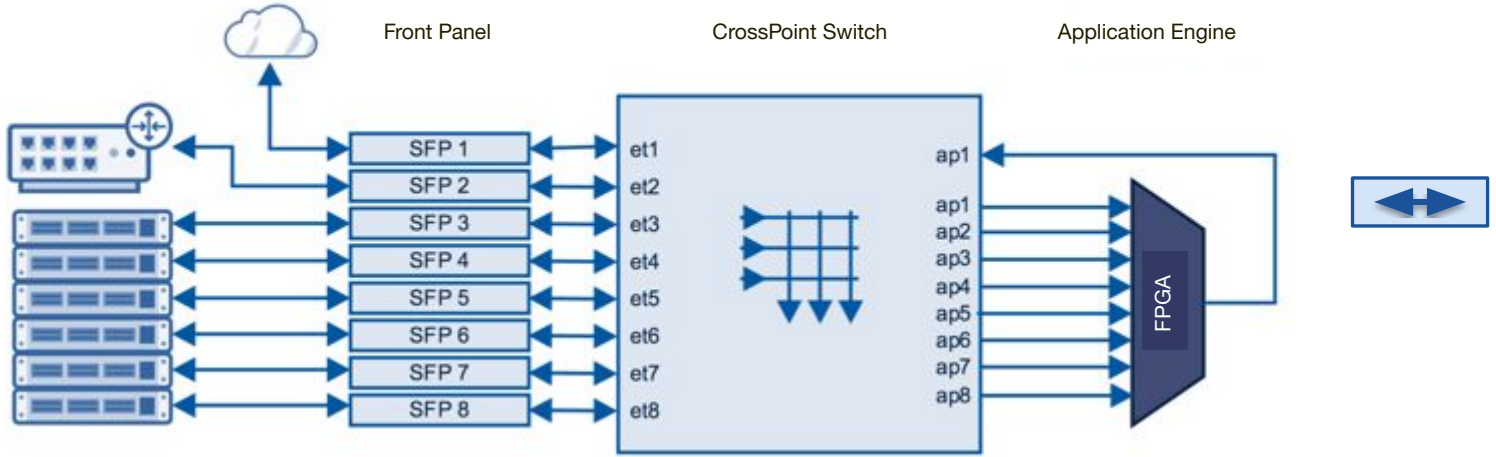
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Arista 7130: MetaMux



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MetaMux Configuration - FPGA Connectivity



Market Data – In	Executions - MUX	Executions - MUX	Executions - MUX	Executions - Out
Int Et1 Destination Et2,Et3,Et4,Et5, Et,6,Et7,Et8	Int Ap2 Source Et2 Int Ap3 Source Et3 Int Ap4 Source Et4	Int Ap5 Source Et5 Int Ap6 Source Et6 Int Ap7 Source Et7	Int Ap8 Source Et8	Int Et1 Source Ap1

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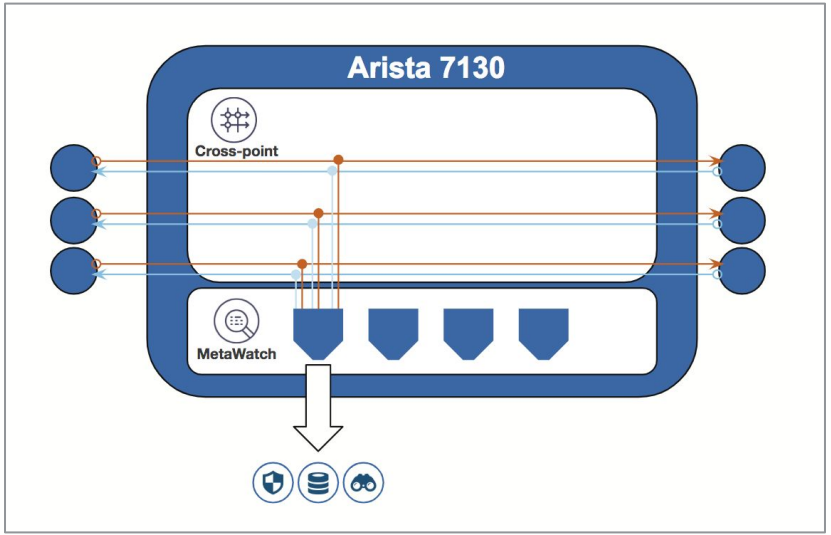
MetaWatch

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Arista 7130: MetaWatch

Summary

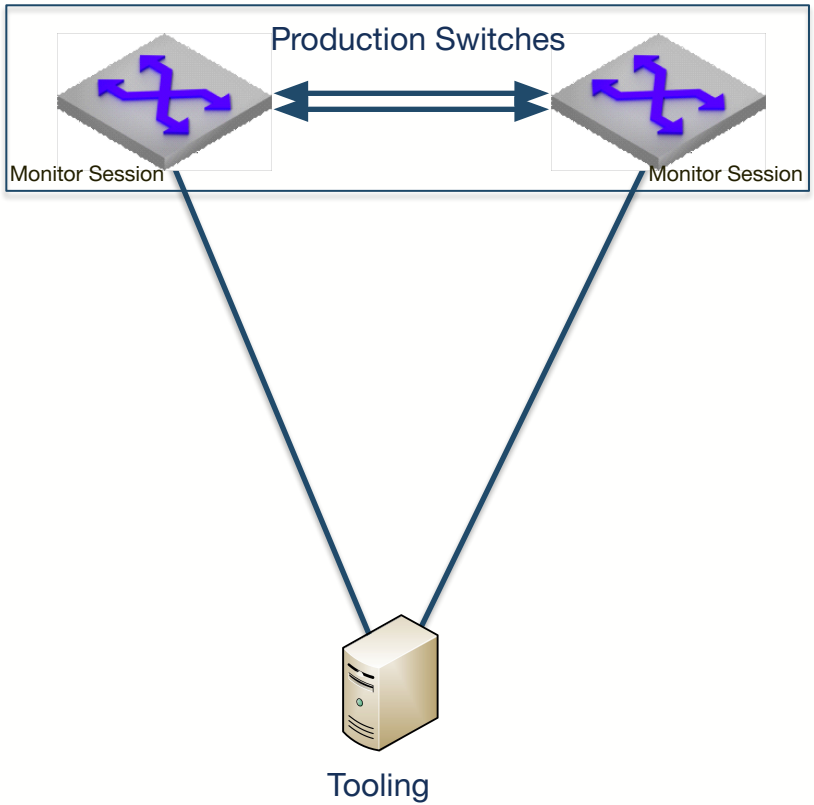
- Tapping
  - Minimal performance impact
- Multiport capture and aggregation
- Precise time synchronization
  - PTP, NTP, PPS input
  - OCXO standard with Atomic clock option
  - Sub-nanosecond accurate timestamping
- Advantages
  - L1 Signal regeneration and stats
  - 4 x 12 in -> 1 out aggregation
  - Deep buffering with 32GB and stats
  - Absorb back-pressure from consumers



Optimized for Arista L Series
Supported on Arista L and K Series

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How Do We Replicate Data out of the Network?



Monitor Sessions

+ Simple to configure

+ No additional hardware required

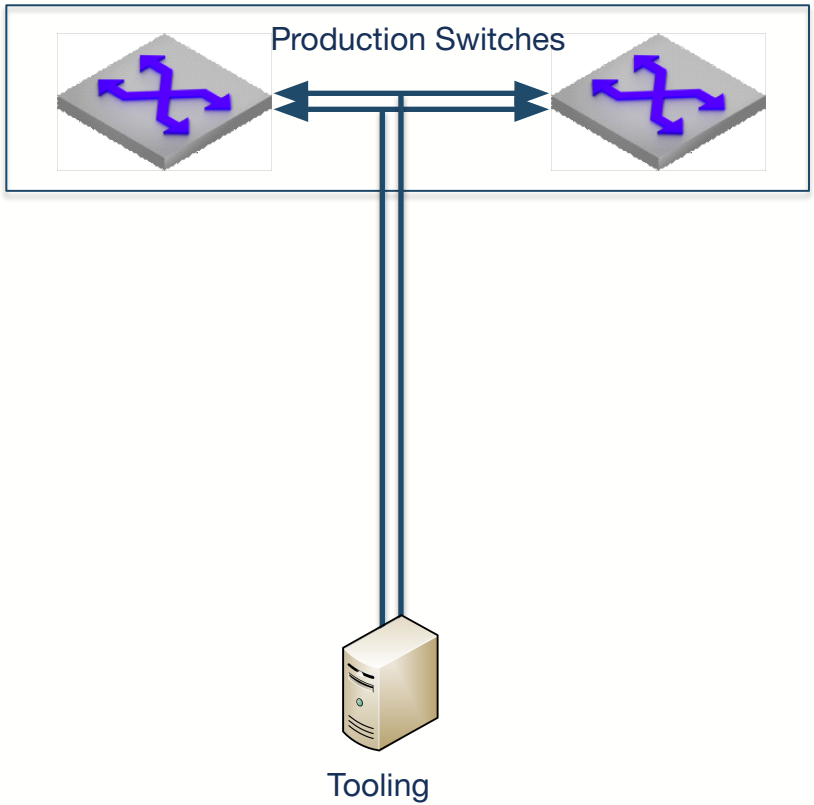
- Indicative data, not absolute. Traffic seen/missing on monitor session port doesn't mean the same is true on the production interface

- Risk to production traffic, shared buffers, scheduler

- Often limited/no timestamp capability

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How Do We Replicate Data out of the Network?



Optical TAPs

+ Capture real ‘on the wire’ traffic

+ Introduces fairly small accuracy skew (+/- 5ns)

- Requires ‘splitting’ the power of an optical signal between two links (usually 60/40)

- Risk to production traffic, though link flaps and increased CRC/PCS errors

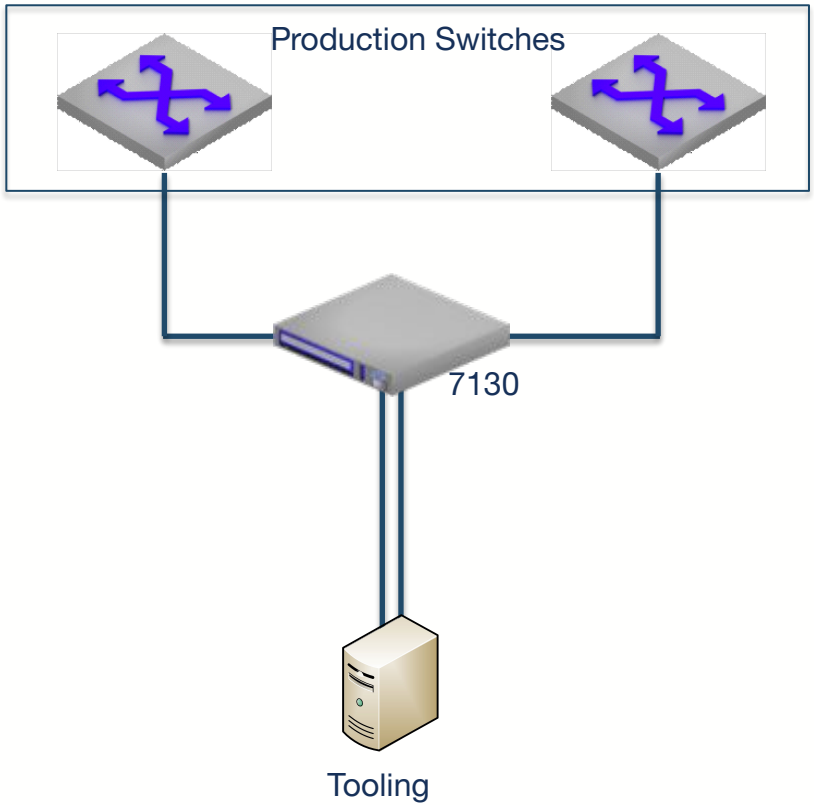
- No data/telemetry on link performance / error rates

- Potential to create grey failures

- High density taps deployments create a large number of distributed cables to manage

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Arista 7130 Series running MetaConnect



Active Tap Patch Panel

+ Provides a physical aggregation point for large volumes of cabling

+ Retimes and boosts signals, both production and replicated links will have 100% signal strength

+ Interface measurement, counters and statistics to provide visibility of link performance

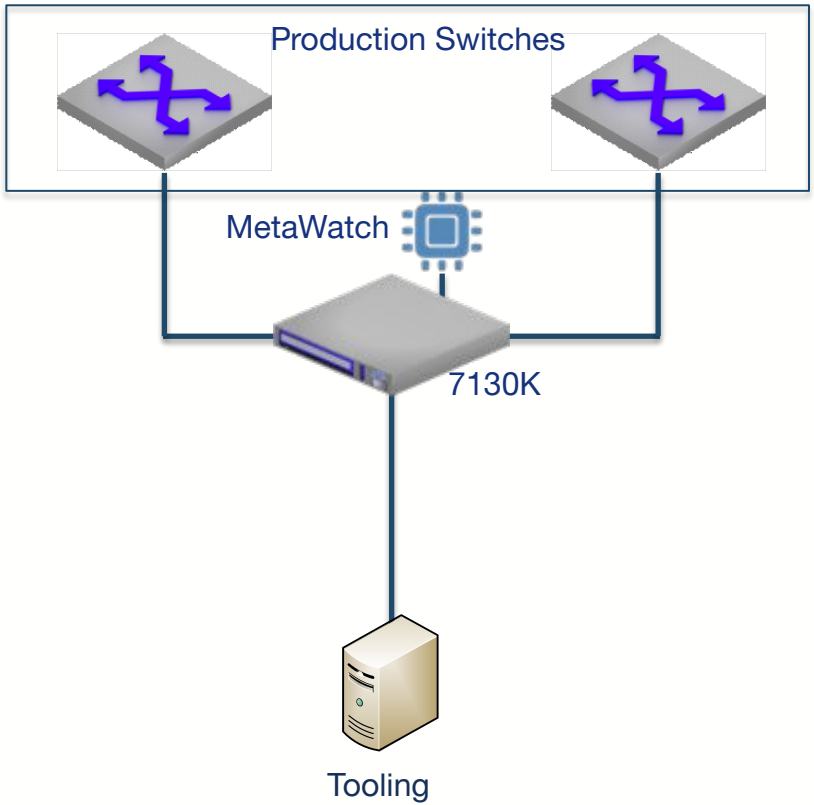
+ Support for dynamic reconfiguration of links, allowing ‘on demand’ tapping of the whole network with minimal investment.

- Each Bidirectional TAP requires 4 ports (2 prod, 2 mirror)

- Introduces an active device to failure path

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Arista 7130K Series running MetaWatch



Active Tap Patch Panel & Concentrator

+ Shares all of the benefits of MetaConnect

+ Supports N:1 mapping rather than 1:1, reducing the number of ports required per tap

+ Provides deep buffers (8/32GB) to ensure data isn't dropped on the aggregation interface

+ Optionally appends pico secon full UTC timestamps to mitigate transit delay from buffering

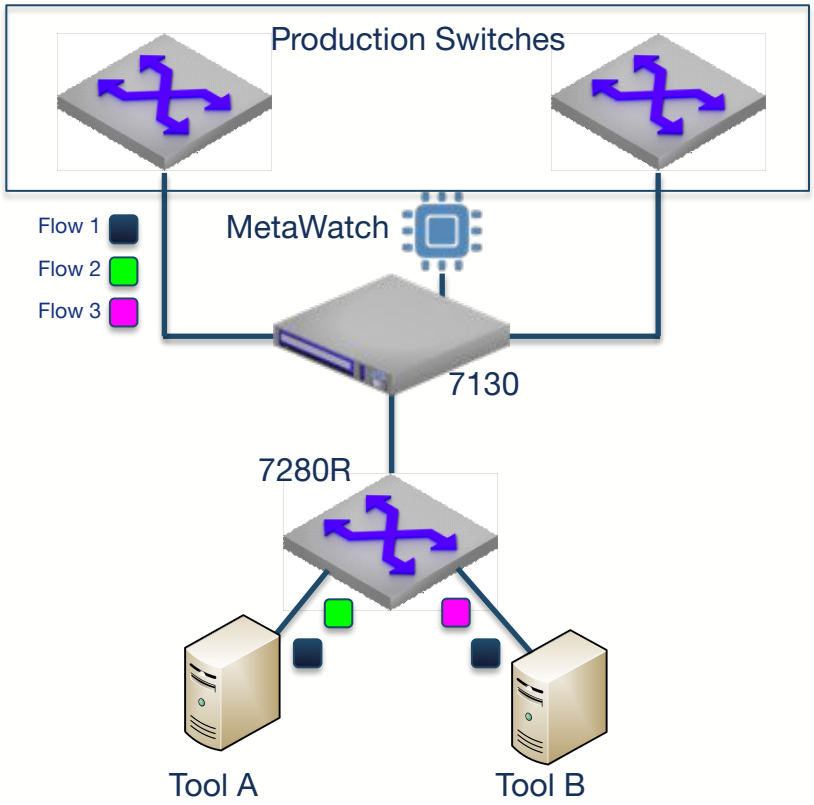
+ Time is synced via either PTP/NTP and PPS

- Introduces an active device to failure path

- All traffic is aggregated from 1 – 4 non-filtered FPGA interfaces

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Arista MetaWatch & 7280R



Dynamic Capture Infrastructure

+ Shares all of the benefits of MetaWatch

+True N:M Mirroring

+Scale out to multiple tools

+ 7280R layer enables flow based traffic steering capability

+ 7280R layer provides support for L2-L4 based filtering functions

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MetaWatch Logic

- Logically similar to Mux
- Production Packet is forwarded in 5ns over the cross point. A copy of this packet is replicated to the FPGA for time stamping.
- MetaWatch supports capture of up to 28 1GbE, 48 10GbE or 7 40 GbE ports depending on platform

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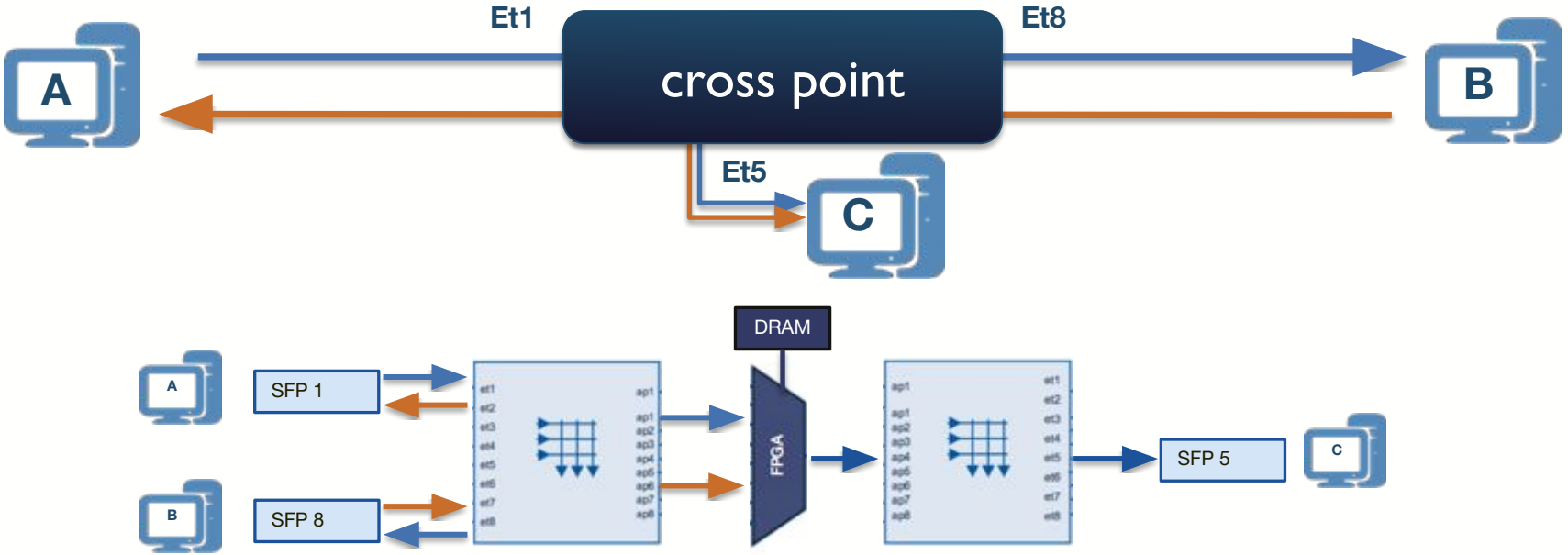
Arista 7130: MetaWatch Timestamp Format

Timestamp format - Metawatch Ethernet Trailer

- Port ID
- Device ID
- Bit flags
  - FCS valid
  - Extensions present flag
- Seconds / Nanoseconds since epoch (in UTC)
- Sub-nanoseconds (optional - extension)
- Sequence Number (optional - extension)

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MetaWatch Logical Path



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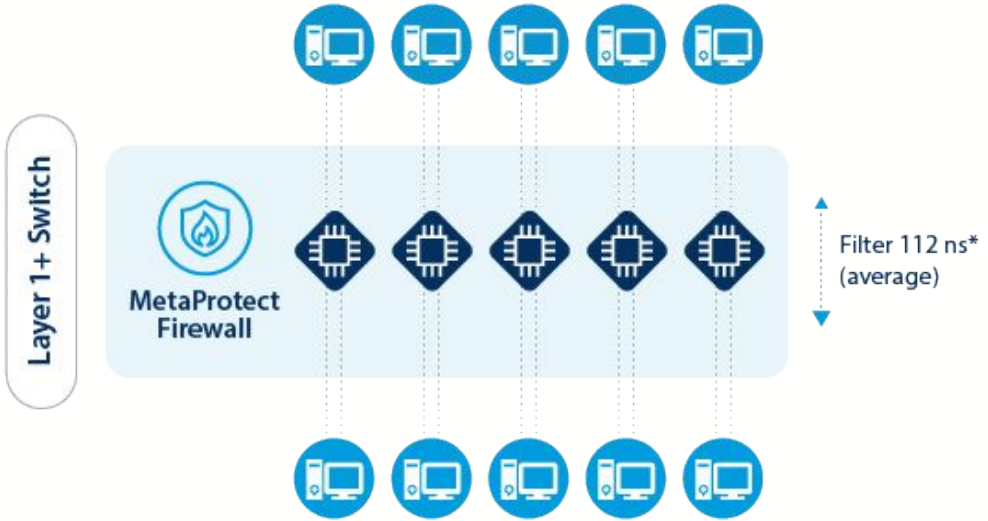


MetaProtect

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MetaProtect: Low Latency Packet Filtering

- Secure Stateless ACL Appliance
- 110ns latency for filtered traffic
- 48 * 10GbE SFP+ ports
- Integrated L1 switch
- L3/L4 Filter definitions
- Cut through filters
  - 32 ACLs up to 510 rules
- Logging
- Port Statistics



7130-P48C: Arista 7130 Series Protect Firewall 48

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MetaProtect – Forwarding Details

- Delayed Cut-through (Packet not forwarded until a decision has been made, but typically before whole packet has been received). [Roadmap]
  - If denied, packet header is logged to file.

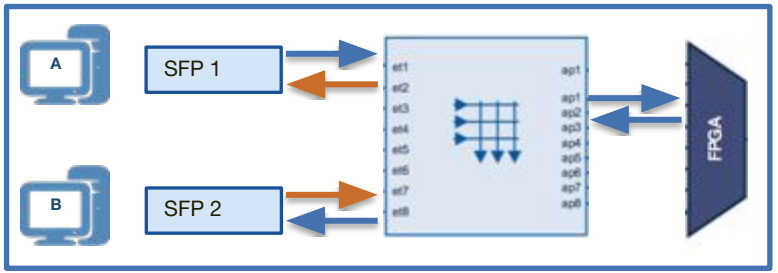
- Latency defined by the logic of the firewall rules
  - How many ACEs exist in the applied ACL
  - Where in the header the match criteria exists, i.e L3 or L4 Header
    - Best Case Match IP any any (110ns)
    - Worst Case 510 rules which involve destination port matching (190ns)

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MetaProtect Logical Path

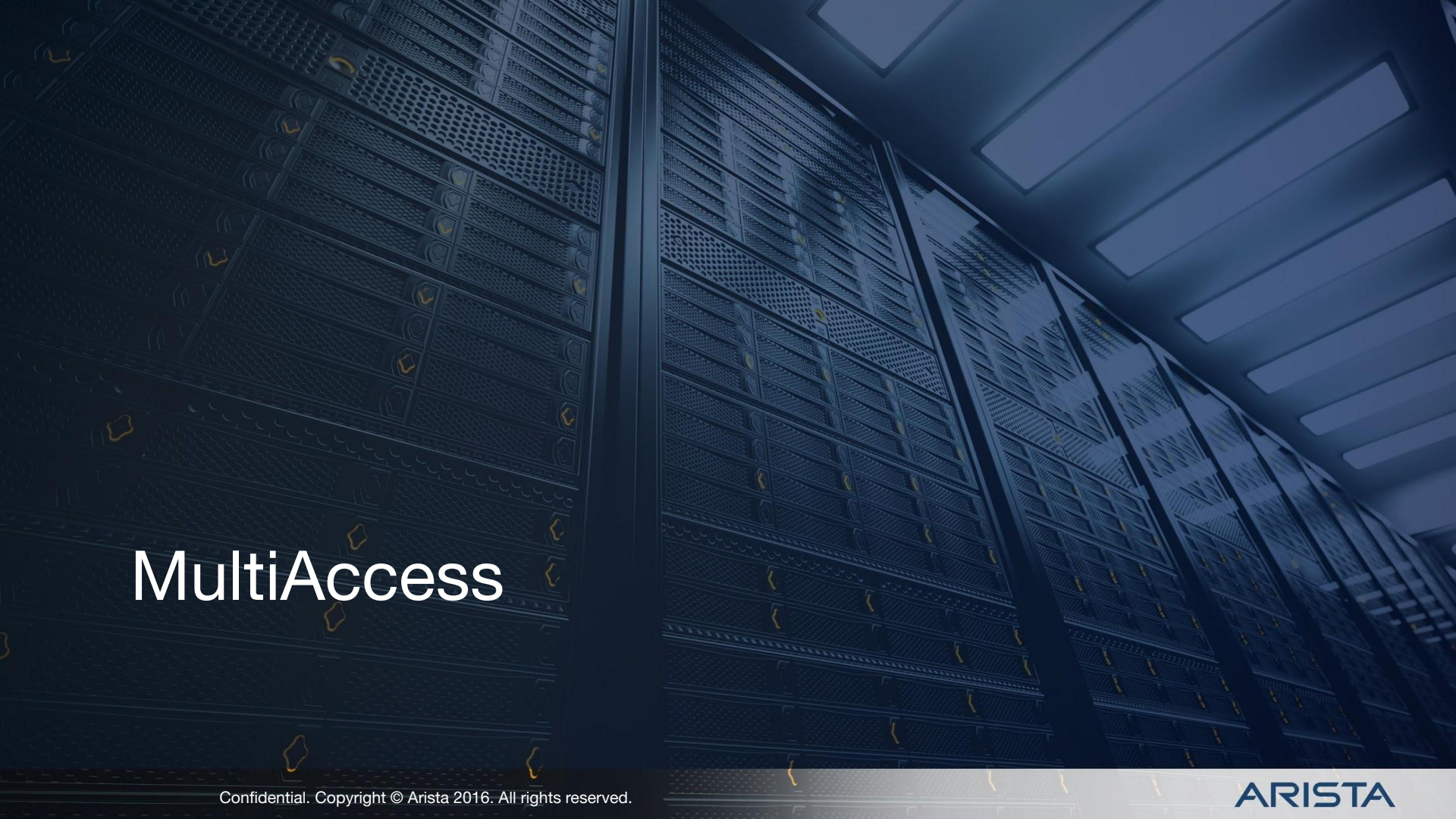



```
hostname(config)> int et1
hostname(config-if-et1)> destination ap1
hostname(config-if-et1)> source et2
hostname(config)> int et2
hostname(config-if-ap1)> source ap1
```



NOTE: Destination command on Et1, is really a ‘Source Et1’ command on Ap1

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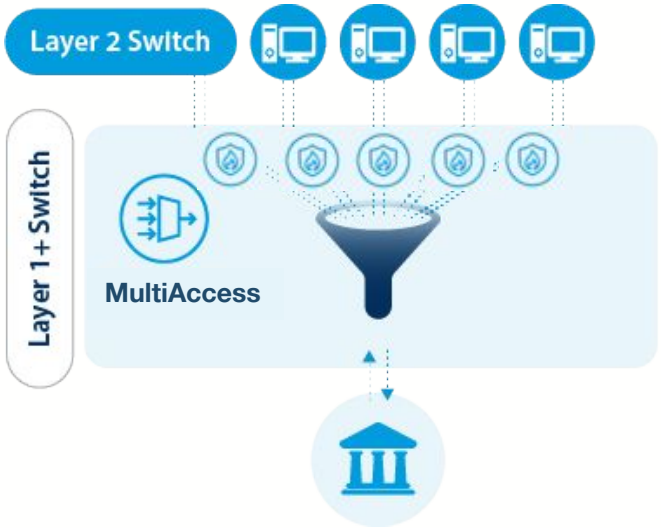
MultiAccess

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MultiAccess: Multi-tenancy

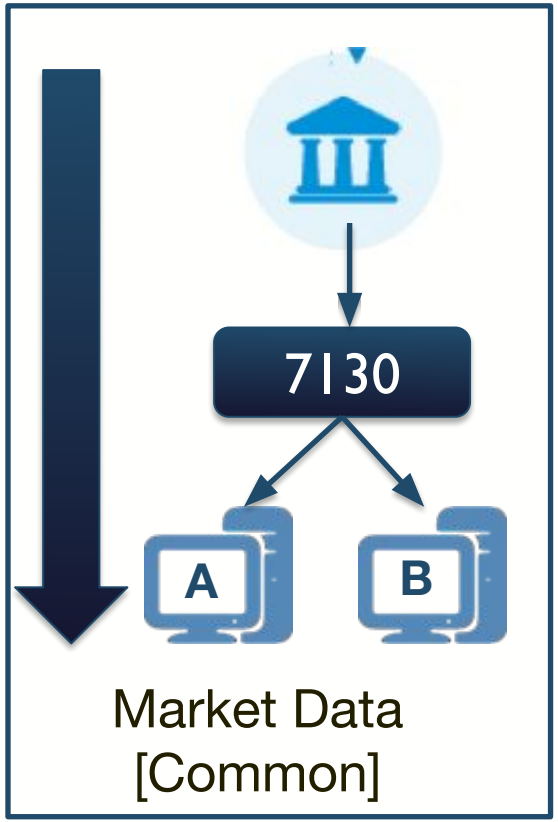
- Designed for service providers or brokers
- Share a single connection between multiple firms
- Combines Muxing and Filtering into a single application
- Different modes for different use-cases

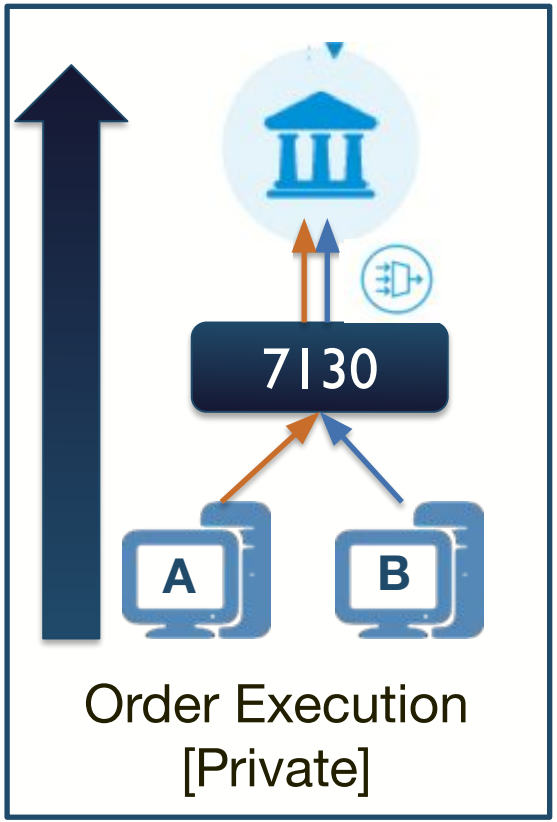


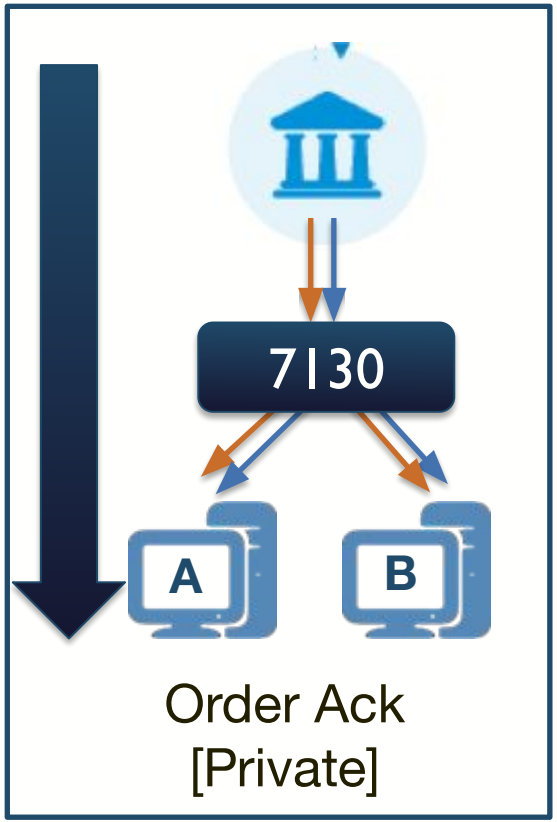
7130-48E: Arista 7130 Series 48E with UltraScale KU095 FPGA
7130-96E: Arista 7130 Series 96E with UltraScale KU095 FPGA

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MultiAccess – Three Elements of a Trade

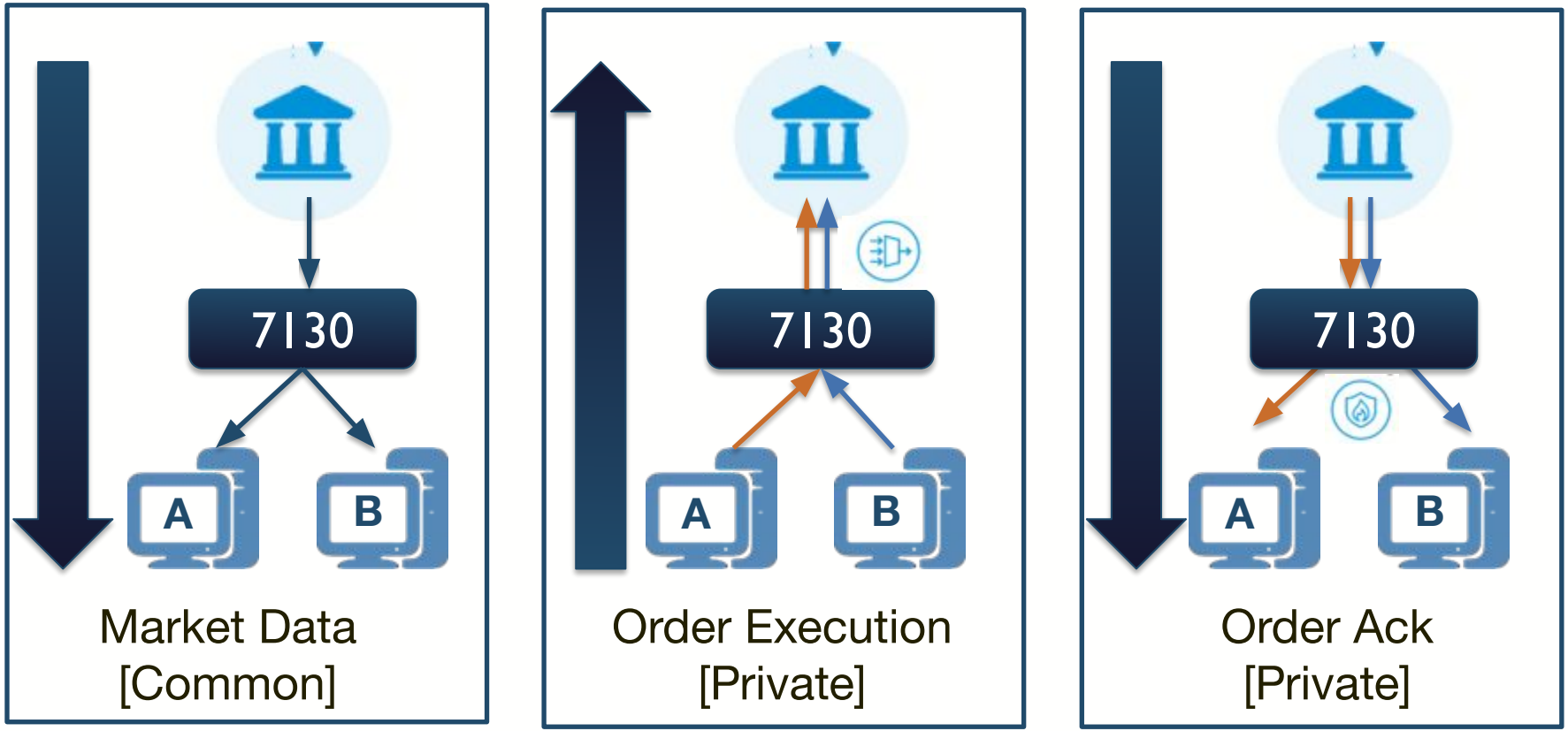






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MultiAccess – MUX and Filter

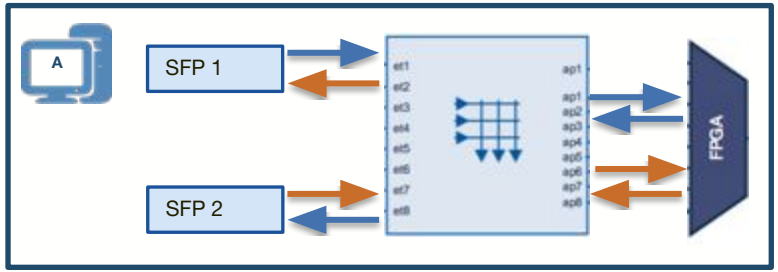


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MultiAccess Logical Path




```
hostname(config)> app multiaccess
hostname(config-app-multiaccess)> connect multiaccess-group 0 client 0 et1
hostname(config-app-multiaccess)> connect multiaccess-group 0 server et2
```



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MultiAccess – Extra Features

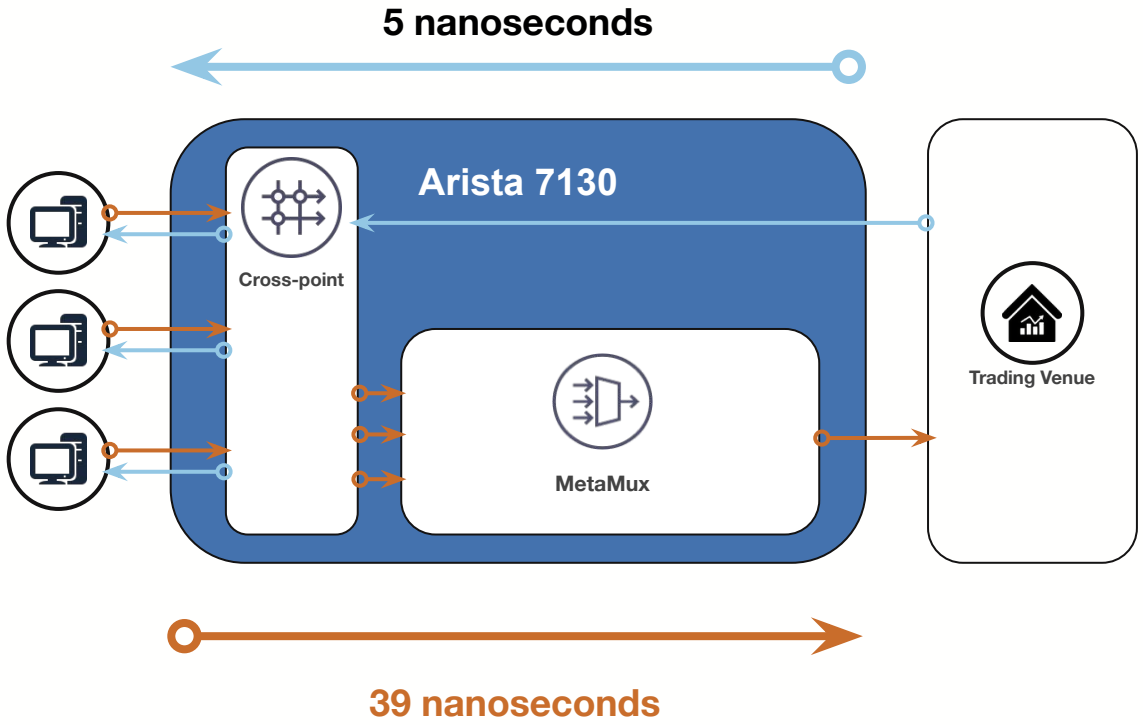
- Telemetry
  - By default all counter statistics are logged to a local influxdb time series data base
  - Stats can be accessed remotely using Telemetry View or exported to another influxdb instance
- Server Port Speed
  - In addition to 10G support, server/exchange facing interfaces also support 1G.
- Simplified Configuration
  - MultiAccess can be configured with the standard source/destination commands or using the ‘connect multiaccess group’ command

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Use Cases

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Arista 7130: Low Latency Switching



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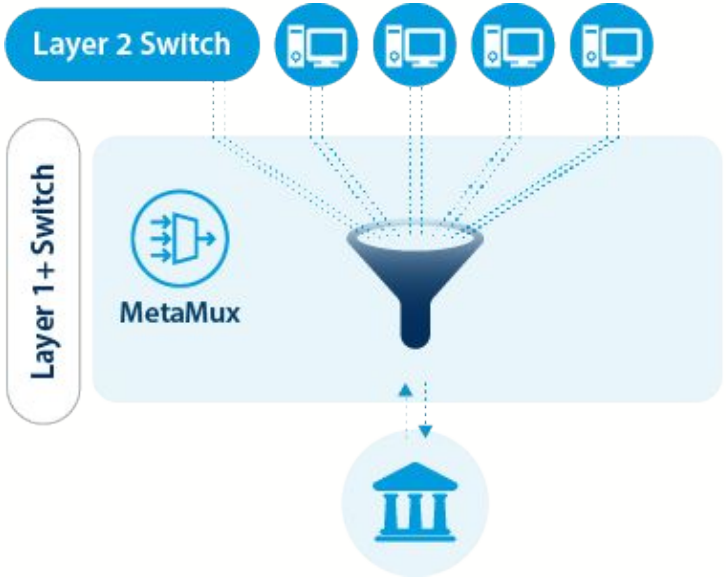
Trends in Electronic Trading

- Market consolidation has increased latency competition
- The “race to zero” continues…
- Layer 1 networking now mainstream
- Hardware-driven strategies with FPGAs
- Improved exchange determinism
- Latency-optimized microwave radios
- Precomputation with GPUs/TPUs
- Precision monitoring & timestamps

< 1µsec
Tick-to-trade time

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Low-latency exchange connectivity

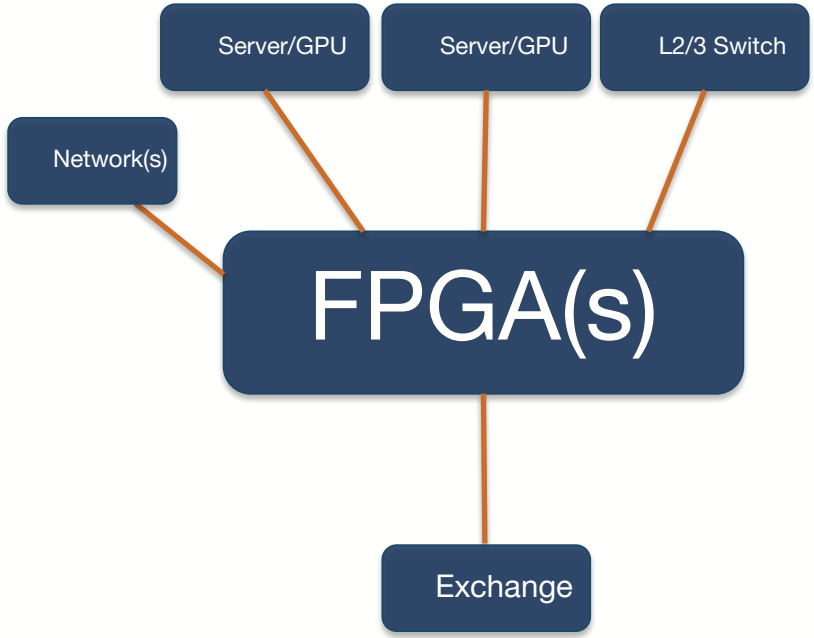


- Layer 1 replication for incoming market data
- FPGA-based multiplexing for order entry
- 100s of ns of latency savings over traditional L3 edge-switches
- No address lookups - reducing jitter
- Layer 1 features include …
  - packet statistics, signal regeneration, dynamic patching, tapping and more
- Configurable size and number of Mux instances

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HFT Algorithm Deployment, FPGA based trading

- FPGAs can respond in < 200 ns
- For FPGA-based trading, single-digit nanoseconds matter. *Any* switching latency is too high.
- Fiber latency *is* significant
- Still need monitoring and timestamping
- Solution: deploy custom trading algorithms to the FPGAs inside the switch – connect direct to the market.
- Result: minimal fiber latency in adjacent rack units, no switching latency, monitoring features.
- Pass through via muxing of insensitive traffic.

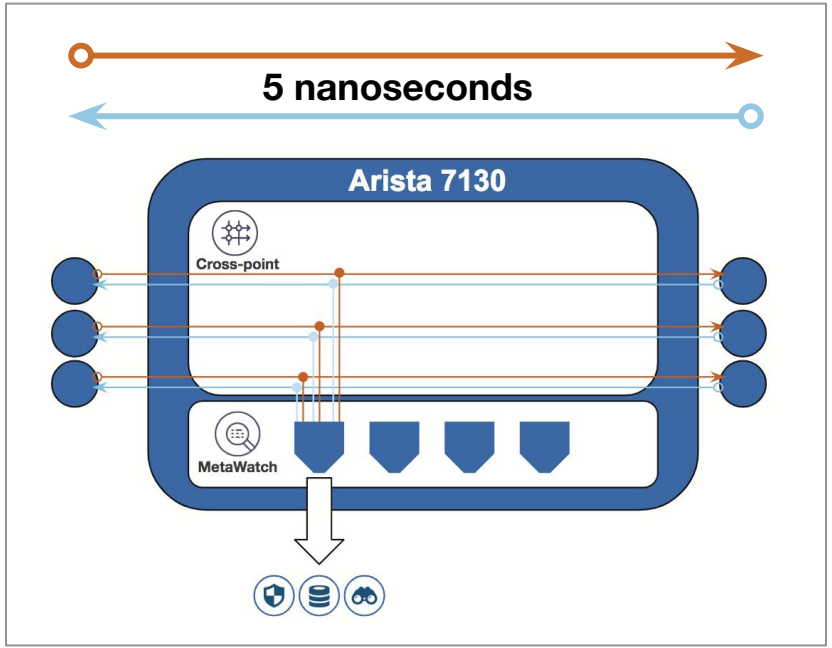


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Arista 7130: **MetaWatch** - Tap Aggregation

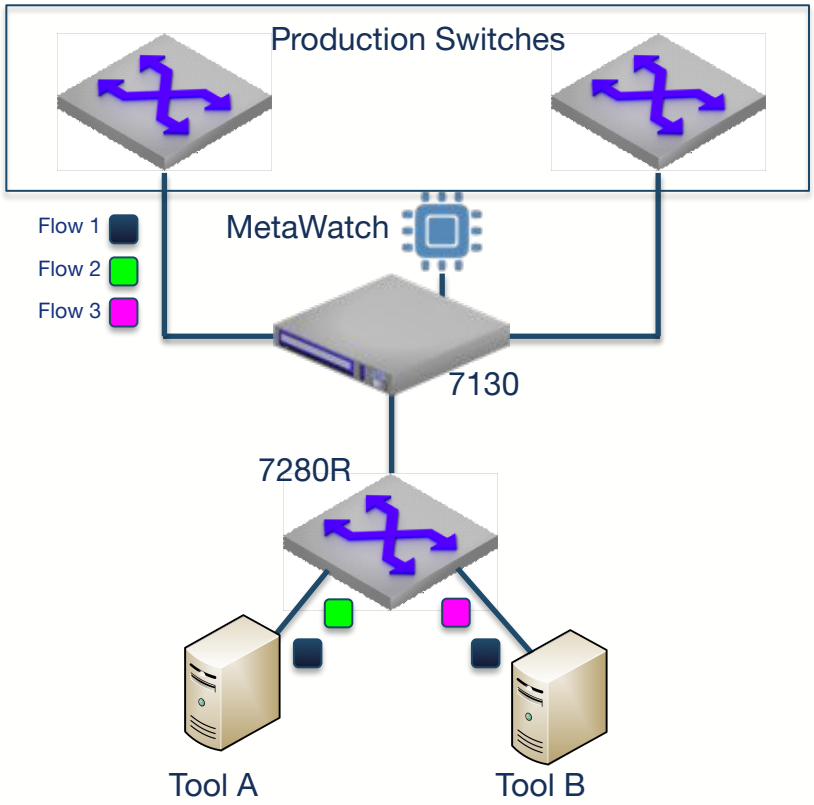
Advanced network monitoring

- Tapping
  - Minimal performance impact
- Multiport capture and aggregation
- Precise time synchronization
  - PTP, NTP, PPS input
  - OCXO standard with Atomic clock option
  - Picosecond accurate timestamping
- Advantages
  - Signal regeneration
  - L1 and buffer stats
  - 4 x 12 in -> 1 out aggregation
  - Deep buffering with 32GB
  - Absorb back-pressure from consumers



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Arista MetaWatch & 7280R



Dynamic Capture Infrastructure

+ Shares all of the benefits of MetaWatch

+True N:M Mirroring

+Scale out to multiple tools

+ 7280R layer enables flow based traffic steering capability

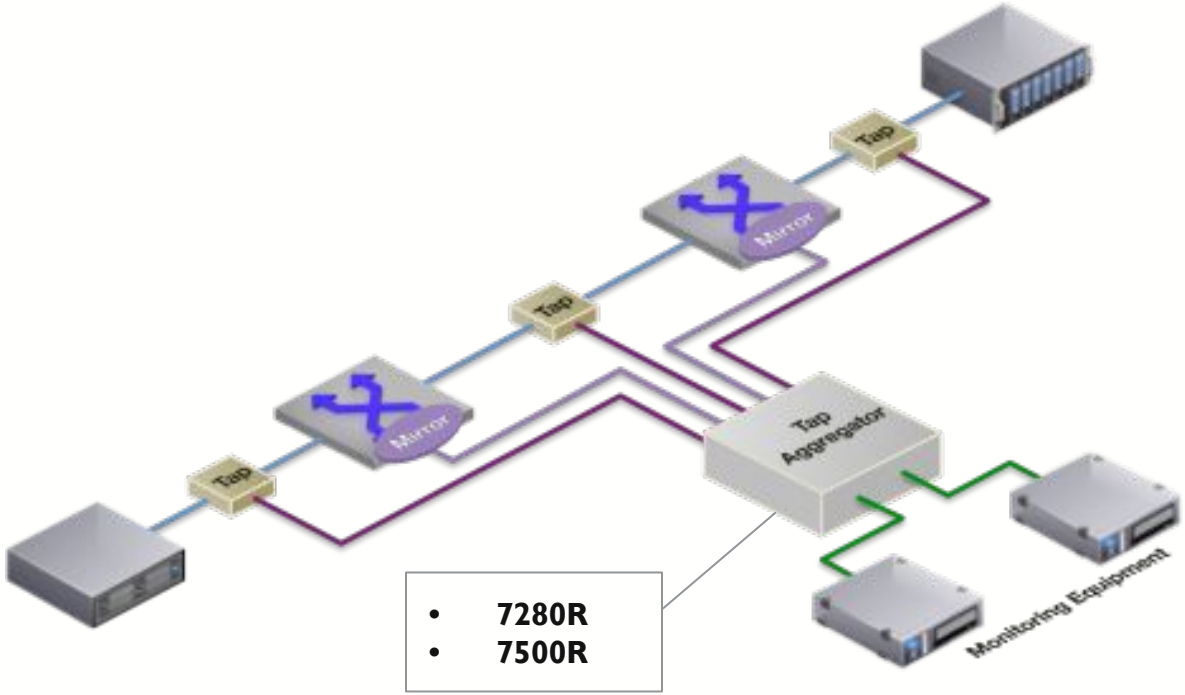
+ 7280R layer provides support for L2-L4 based filtering functions

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Tap Aggregation (7280R / 7500R)

Features:

- Traffic Aggregation
- Signal Regeneration
- Signal Conversion
- Speed Conversion
- Traffic Filtering
- Traffic Steering
- Traffic Marking
- Time Stamping
- Header Stripping
- Truncation / Slicing



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MetaWatch Timestamp Format

- Full UTC 64 bit time stamp
  - 32bit seconds, 32 bit sub second
  - Includes both configurable Device ID and Port ID

```
hostname(config-app-metawatch)Interface et1 source-id 255
hostname(config-app-metawatch)device-id 1234
```

  - Appends a new FCS
  - Support for OXCO or Atomic Clock

- Time stamp is calculated as the packet ingresses the FPGA
  - 15.6 Picosecond accuracy, propagation time of internal board traces is offset.
  - Timestamp is applied as an additional frame trailer, starting at (and maintaining) the original FCS.

- Capacity to add custom Timestamp TLVs with additional data

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Arista 7130: MetaWatch Timestamp format

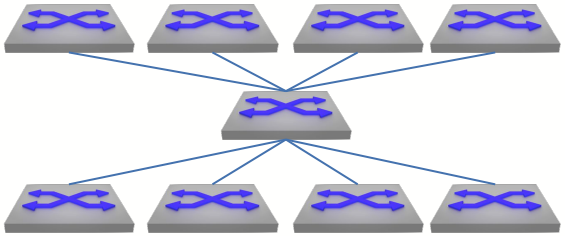
No.	Time	Source	Destination	Protocol	Length	Info
2	0.911310000	65.208.228.223	145.254.160.237	TCP	86	http(80) → tip2(3372)
43	30.393704000	65.208.228.223	145.254.160.237	TCP	122	http(80) → tip2(3372)

```
▶ Frame 2: 86 bytes on wire (688 bits), 86 bytes captured (688 bits)
▶ Ethernet II, Src: fe:ff:20:00:01:00 (fe:ff:20:00:01:00), Dst: Xerox_00:00:00 (00:00:01:00:00:00)
▶ Internet Protocol Version 4, Src: 65.208.228.223, Dst: 145.254.160.237
▶ Transmission Control Protocol, Src Port: http (80), Dst Port: tip2 (3372), Seq: 0, Ack: 1, Len: 0
▼ Metamako ethernet trailer, Timestamp: 11:17:08.222534963, Source Device: 12345, Source Port: 123
    Original FCS: 0xb9e2ec3e
  ▼ Trailer Extensions, Sequence No: 2, Sub-nanoseconds: 0.440881968ns
      Sequence Number: 2
      Sub-nanoseconds: 0.440881968ns
  ▼ Time Stamp: May 13, 2004 11:17:08.222534963 BST
      [Time Difference: 0.000000963 seconds]
  ▼ Flags: 0x02, Has Trailer Extensions
      .... ...0 = Original FCS Valid: Invalid
      .... ..1. = Has Trailer Extensions: True
      0000 00.. = Reserved: 0x00
    Source Device ID: 12345
    Source Port: 123
```

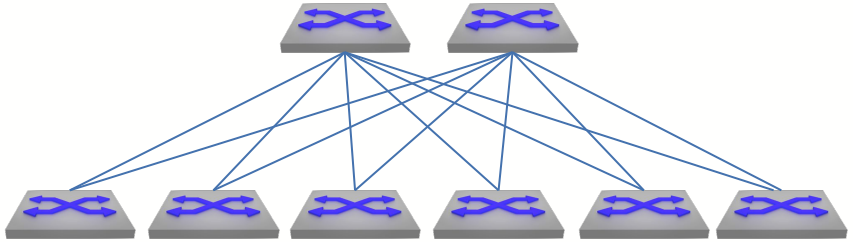

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Dynamic Patch Panel

- A crosspoint works much like a circuit switched network.
- When a connection is configured between A and B they can communicate freely (bidirectionally or unidirectionally).
- If A should instead communicate with C that configuration can be revoked and replaced.
- This for the creation of dynamic point-to-point circuit switched network, ideal for rapid prototyping or lab testing.



Physical



Logical

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Dynamic Topology Matrix - Benefits

- Dynamic reconfiguration of topology via CLI, API or GUI
  - Useful for dynamic ‘intrusion’ networks
  - Useful for lab/dev/test environments
- L1 Matrix means
  - Consistent latency of just 5ns added
  - Effectively a wire, no impact on throughput/performance
  - No trapping of link local frames
  - No potential for a Matrix switch to drop traffic
  - Remote or automated re-configuration reduces need for remote hands
  - Sub-second reconfiguration for high throughput automated testing

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Arista 7130: Statistics & Telemetry

```
S7131#show int counters

Port        RxOctets     RxUcastPkts     RxMcastPkts     RxBcastPkts

---- --------------- --------------- --------------- ---------------

et1        3,935,913          32,075           1,184           4

et2        3,799,069          32,073              79           0

et3            1,988               6               8           0


Port        TxOctets     TxUcastPkts     TxMcastPkts     TxBcastPkts

---- --------------- --------------- --------------- ---------------

et1        3,801,057          32,079              87           0

et2        3,926,427          32,070           1,115           3

et3            9,486               5              69           1
```


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Arista 7130: Statistics & Telemetry

```
S7131#show int et1 counters errors
Port          FCS        Align           Rx        Runts       Giants           Tx
---- ------------ ------------ ------------ ------------ ------------ ------------
et1             0            0            0            0            0            0

S7131#show int et1 counter queue
Port        InDrops
---- --------------
et1               0

S7131#show int et1 counter bins
Port          64 Byte      65-127 Byte     128-255 Byte     256-511 Byte
---- ---------------- ---------------- ---------------- ----------------
et1                8            65450              174                0

Port    512-1023 Byte   1024-1522 Byte    1523-MTU Byte
---- ---------------- ---------------- ----------------
et1                0                0                0
```

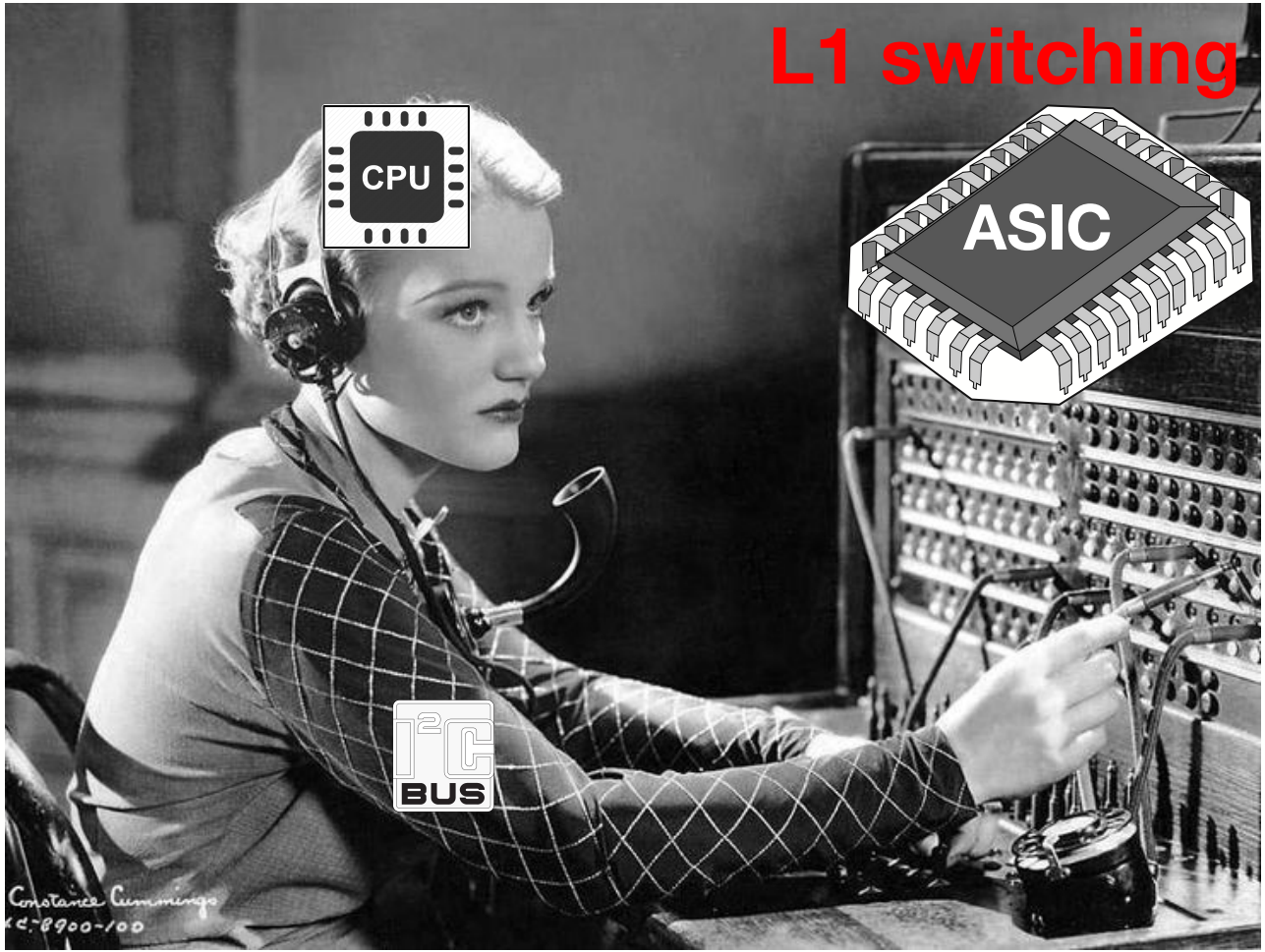

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Arista 7130: Statistics & Telemetry

```
S7131#show int trans
Port Temp (C) Volt (V)  Tx Bias   Tx Pwr   Rx Pwr Status
---- -------- -------- -------- -------- -------- -----------
et1       N/A      N/A      N/A      N/A      N/A
et2     37.19     3.23    32.70    -3.02    -5.83 RS(0),RS(1)
et3     38.43     3.23    31.80    -3.24   -40.00 RS(0),RS(1) RX Power Low

S7131#show lldp neigh
Port Neighbor Device                    Neighbor Port             TTL
---- ---------------------------------- ------------------------- ---------------
et1  s7054.lab.local                    Ethernet64                120 (0:00:20)
et2  s7154.lab.local                    Ethernet16                120 (0:00:20)
```


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